

RYU2-13 CALPELLA UMA Schematics

Intel ULV CPU-Arrandale SFF

Intel Ixex Peak-M

2010-09-28

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REV : A00

DY : Nopop Component

<Core Design>



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

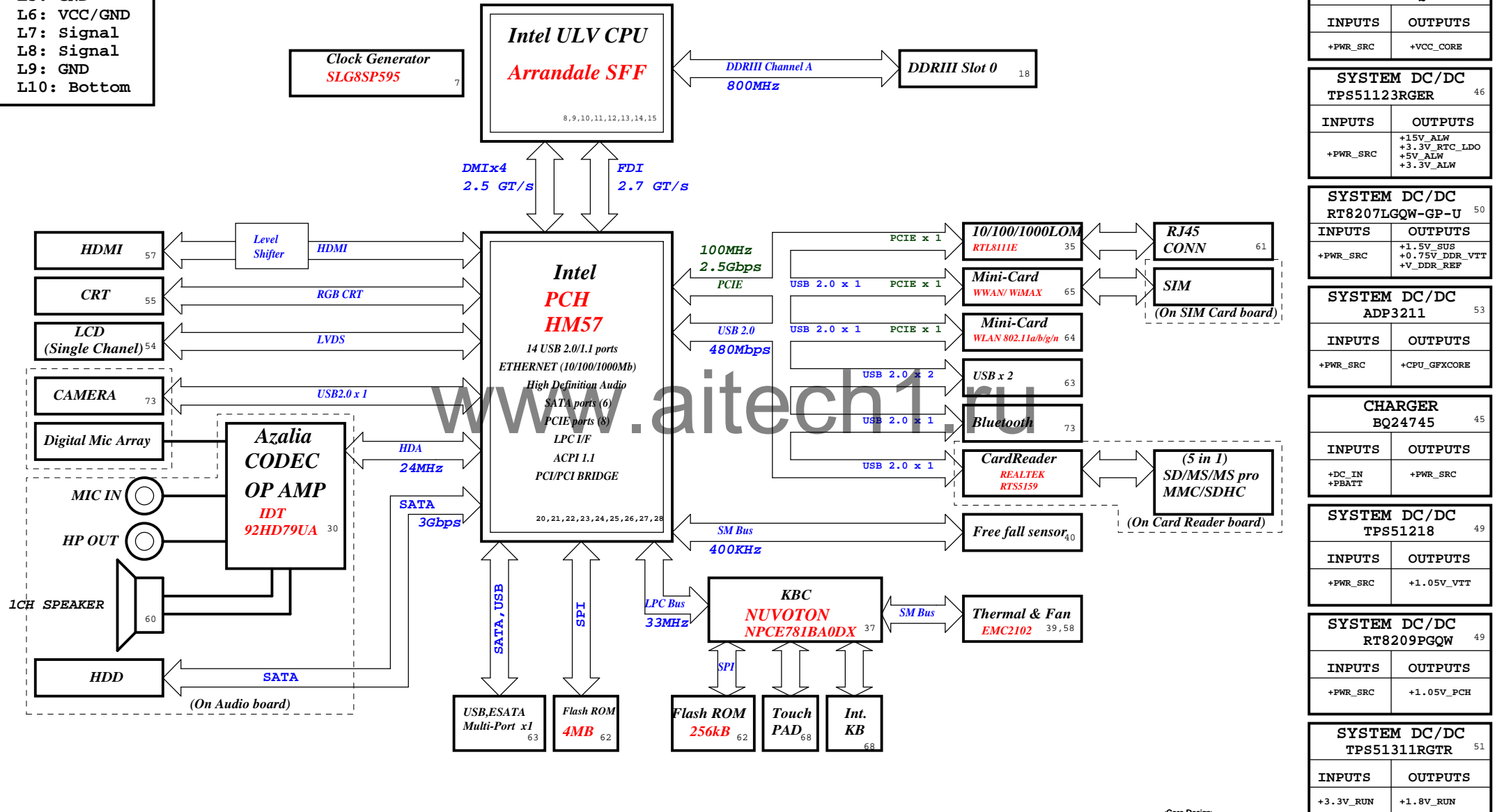
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Cover Page		
Size Custom	Document Number RYU2 13 UMA	Rev A00
Date: Tuesday, September 28, 2010	Sheet 1	of 92

RYU2 CALPELLA Block Diagram

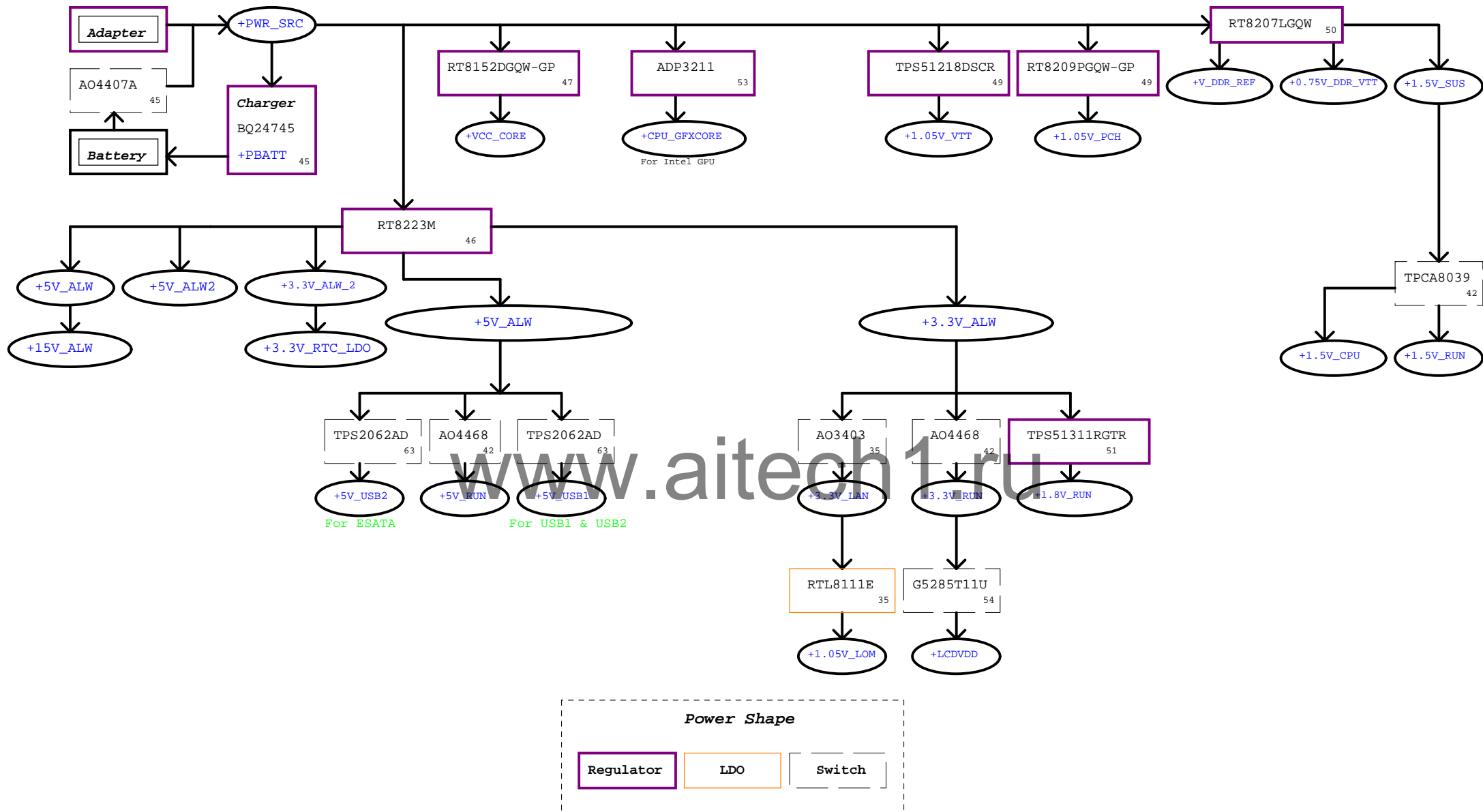
Project code : 91.4M101.001
Part Number : 48.4M101.0SB
PCB P/N : 10251
Revision : SB

PCB LAYER

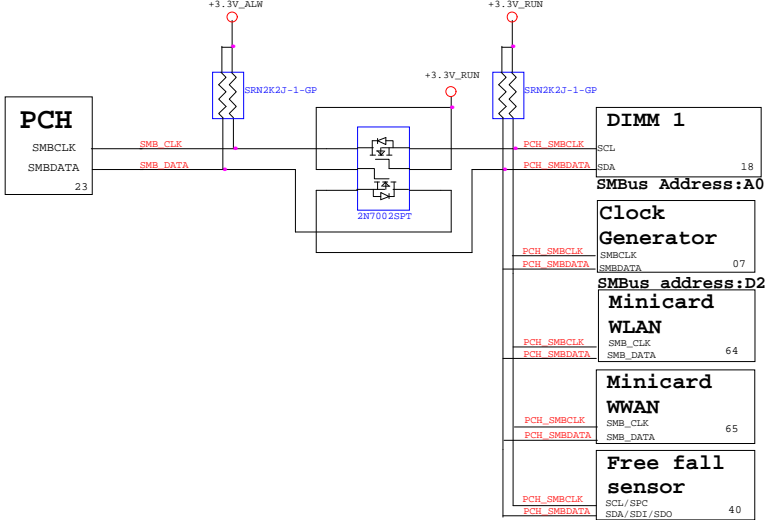
L1: Top
L2: GND
L3: Signal
L4: Signal
L5: GND
L6: VCC/GND
L7: Signal
L8: Signal
L9: GND
L10: Bottom



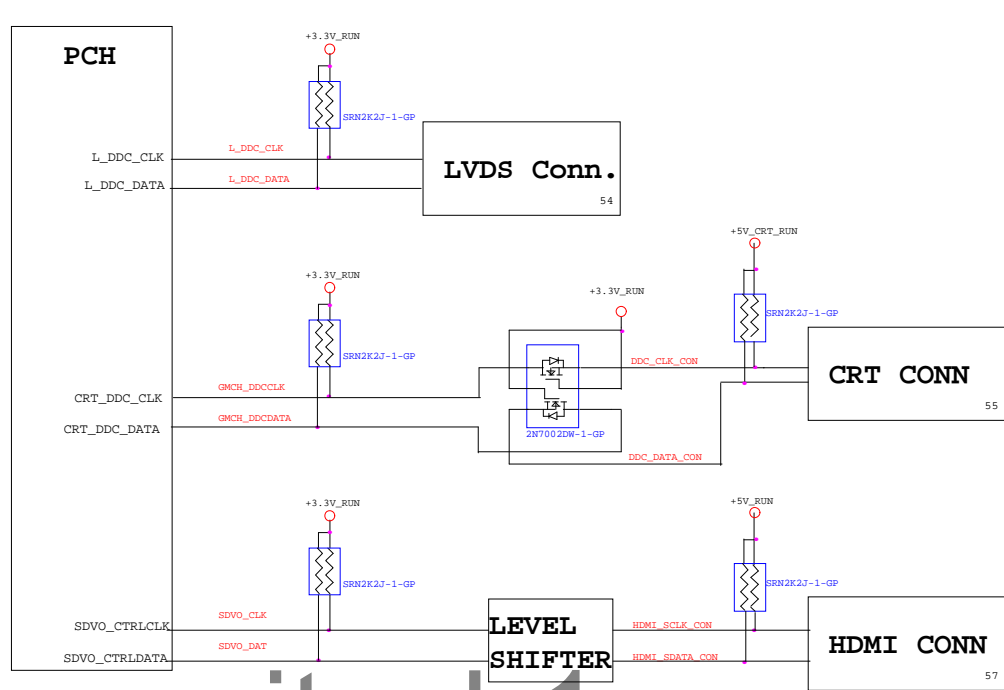
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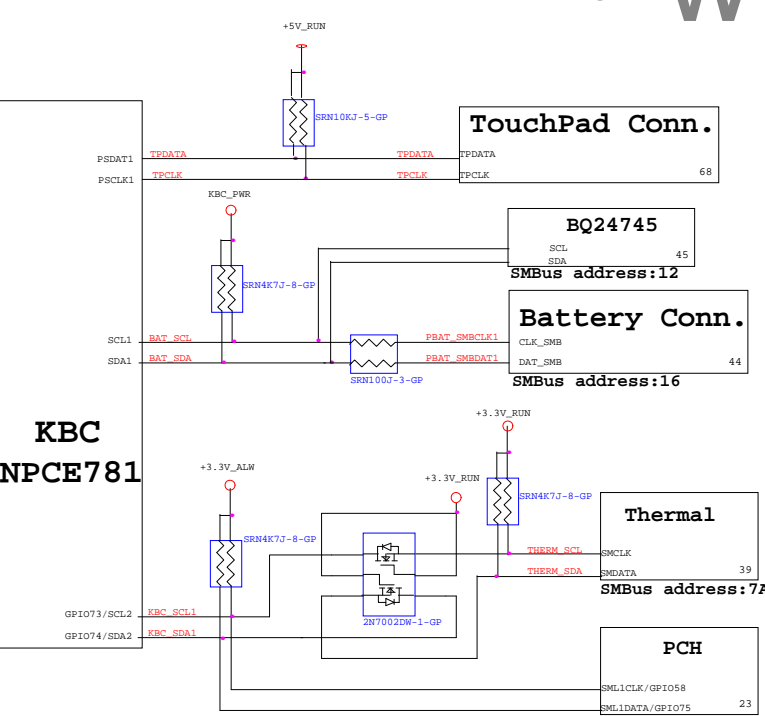
PCH SMBus Block Diagram



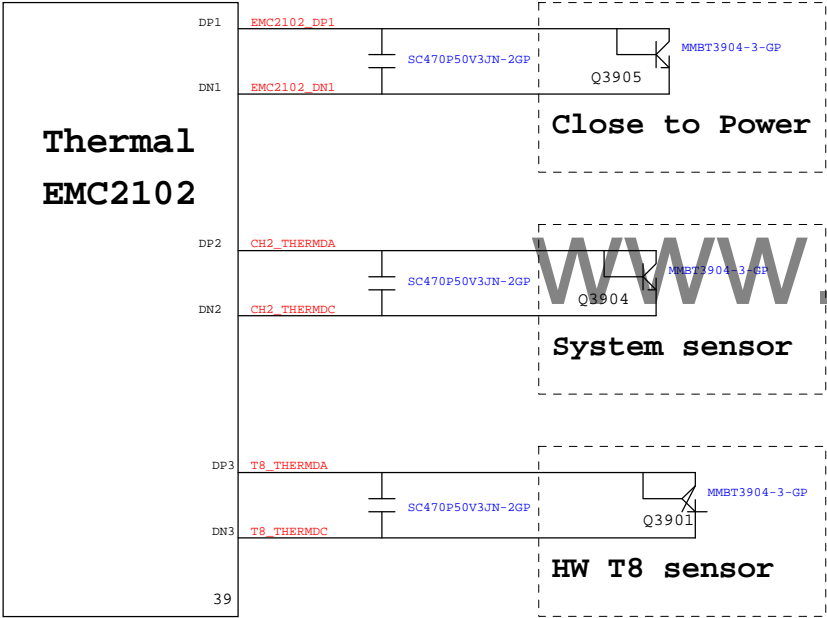
Graphic SMBus Block Diagram



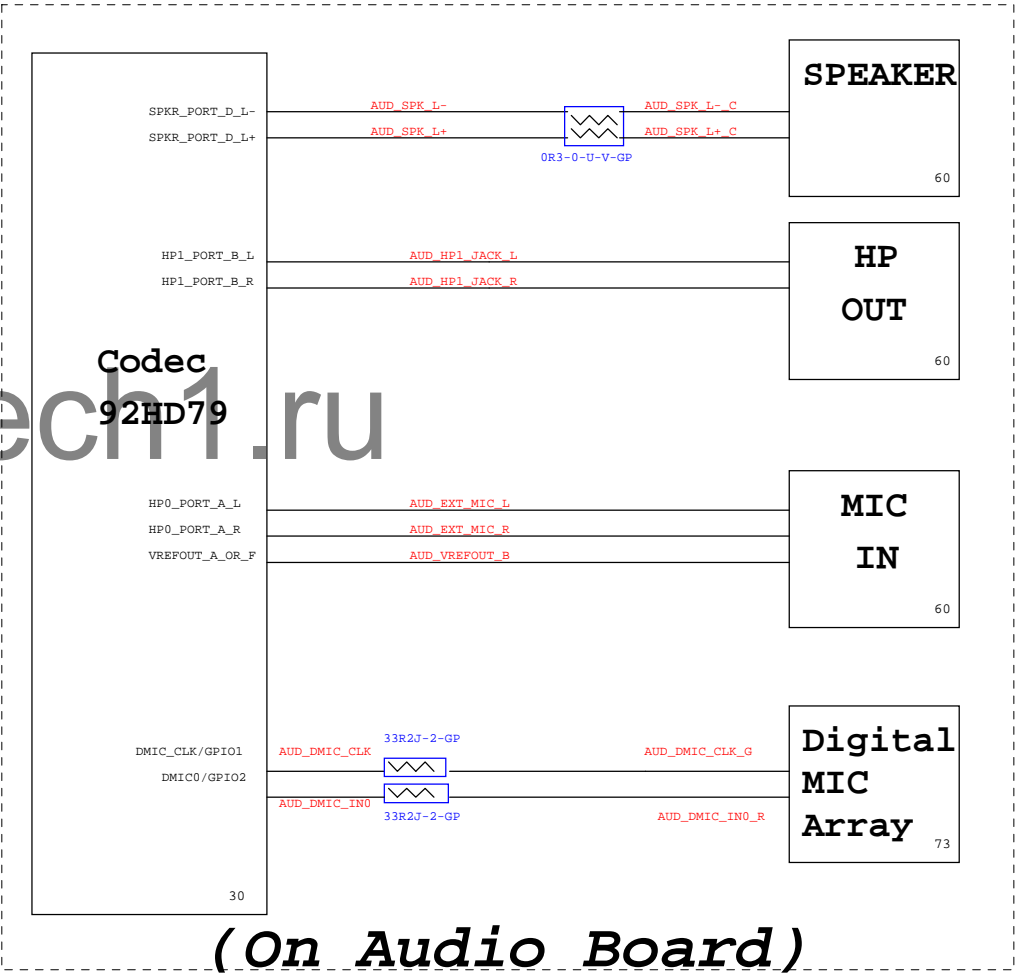
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



PCH Strapping Calpella Schematic Checklist Rev2.0

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor. Intel suggest 1K resistor (Fonseca)
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode Note: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ; do not stuff resistor.
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled Note: CRB uses a 330-kΩ resistor.
GNT0#, GNT1#	Default (SPI): Leave both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.
GNT2#/GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	Enable Intel Anti-Theft Technology: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Intel Anti-Theft Technology: Left floating, no pull-down required.
NV_ALE	Enable Intel Anti-Theft Technology: Connect to +NVRAM_Vccq with 8.2-kΩ weak pull-up resistor.[CRB has it pulled up with 1-kΩ no-stuff resistor] Disable Intel Anti-Theft Technology: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0)- Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1)-: Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (0)- Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1)-: Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note: This is an unmuxed signal. This signal has a weak internal pull-down of 20 KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kΩ pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	Default = Do not connect (floating). Internal pull-up. High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping Calpella SFF Schematic Checklist Rev2.1

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1:Disabled - No Physical DisplayPort attached to Embedded DisplayPort 0:Enabled - An external DisplayPort device is connected to the Embedded DisplayPort	1
CFG[3]	PCI-Express Static Lane Reversal	1:Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 -> 1	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1


PCIE Routing

LANE1	RESERVE
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	RESERVE

USB Table

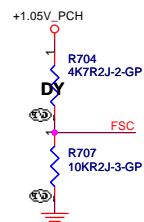
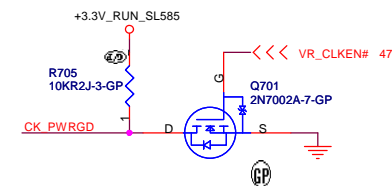
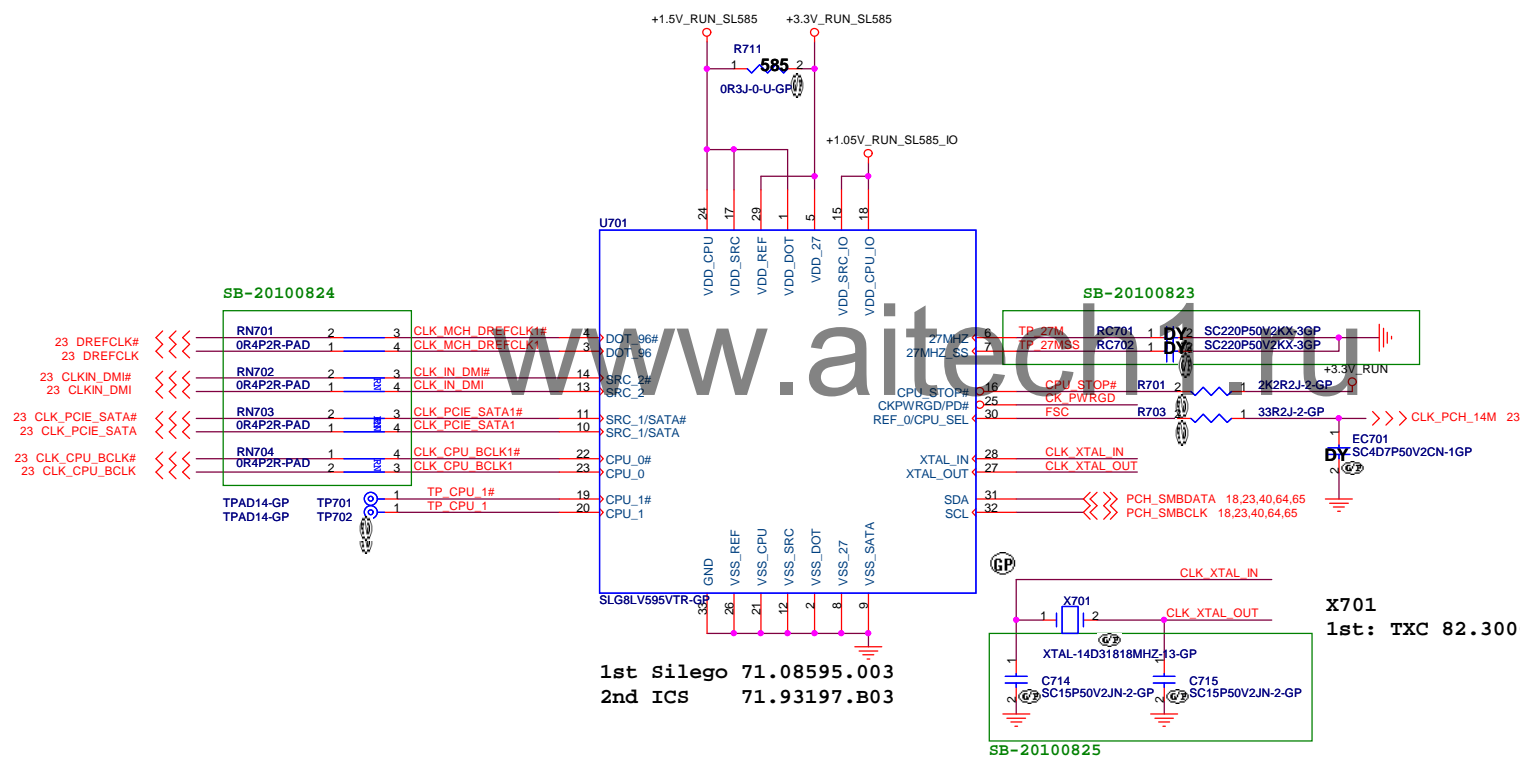
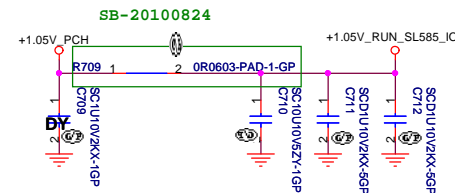
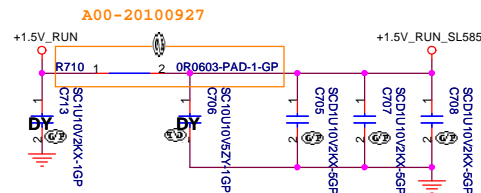
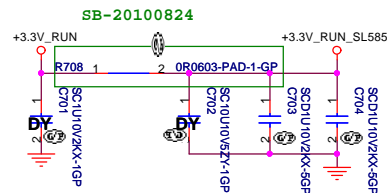
USB	
Pair	Device
0	USB1
1	USB2
2	USB for ESATA
3	RESERVE
4	WLAN
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BLUETOOTH
9	Card Reader
10	RESERVED
11	CAMERA
12	RESERVED
13	RESERVED

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Table of Content			
Size Custom	Document Number RYU2 13 UMA	Rev A00	
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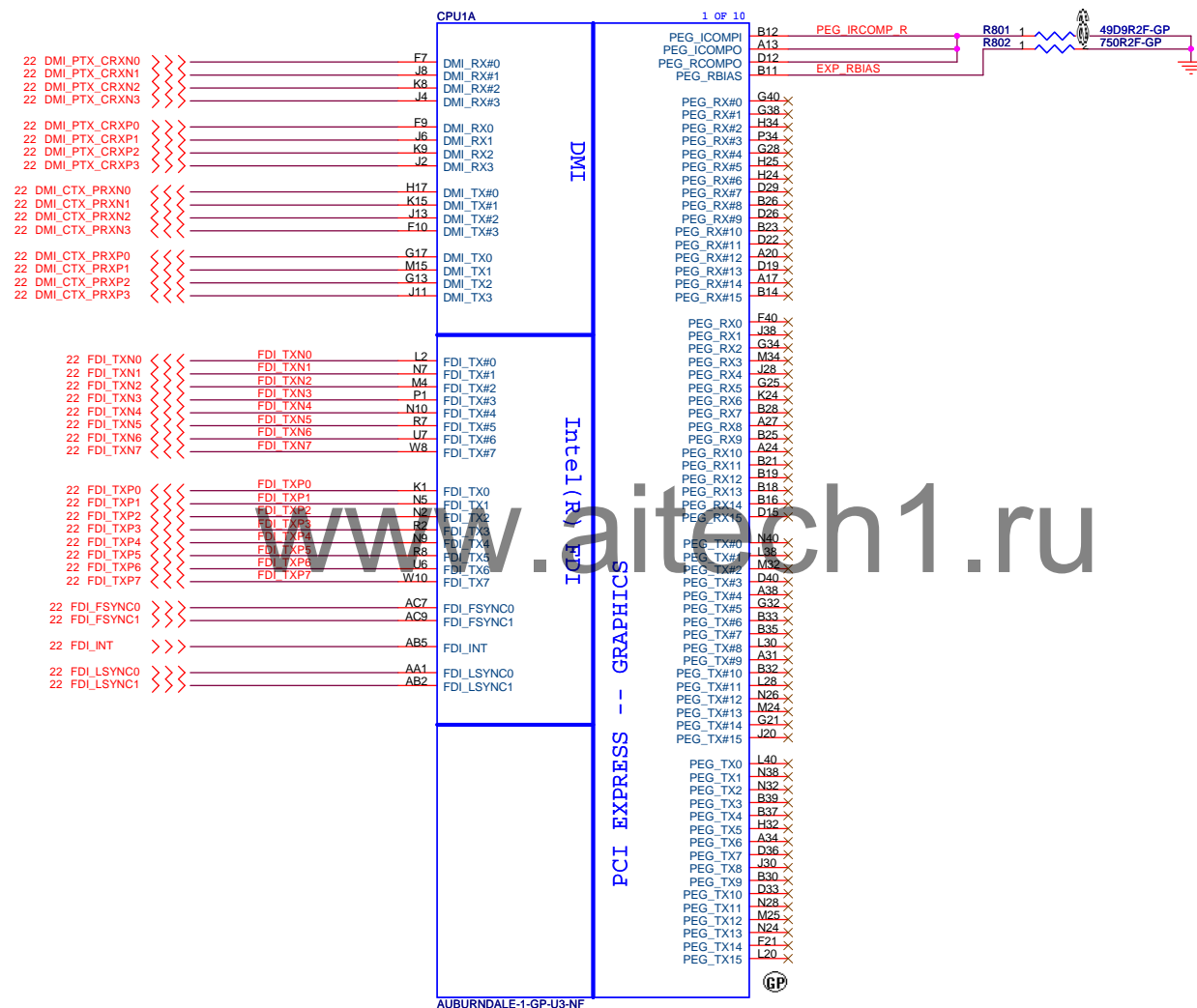
5

SSID = Clock GEN



FSC	0	1
SPEED	133MHz (Default)	100MHz

```
x701
1st: TXC 82.30005.B81
```



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Title

CPU (PCIE/DMI/FDI)-1/8

Size

Document Number

RYU2 13 UMA

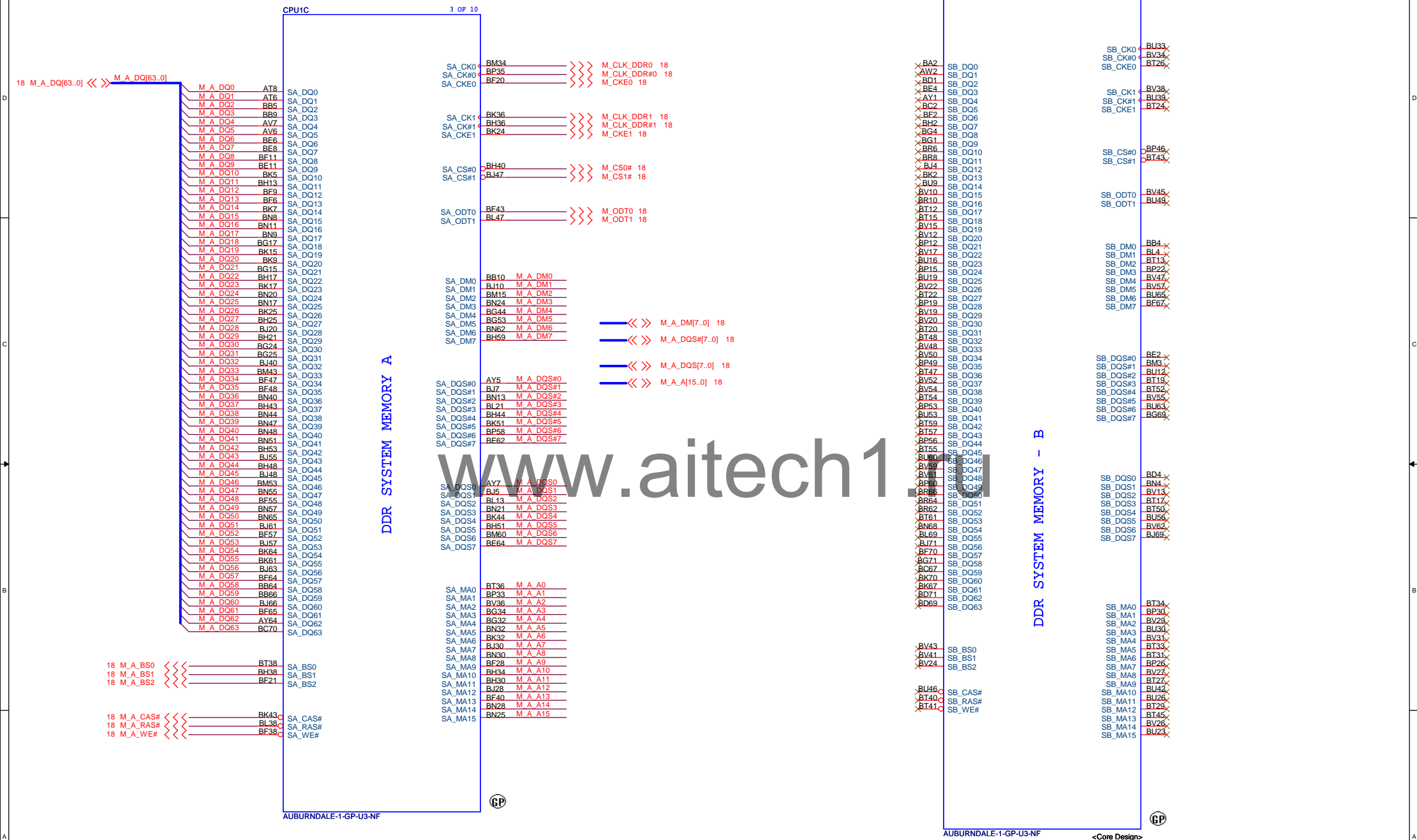
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A00

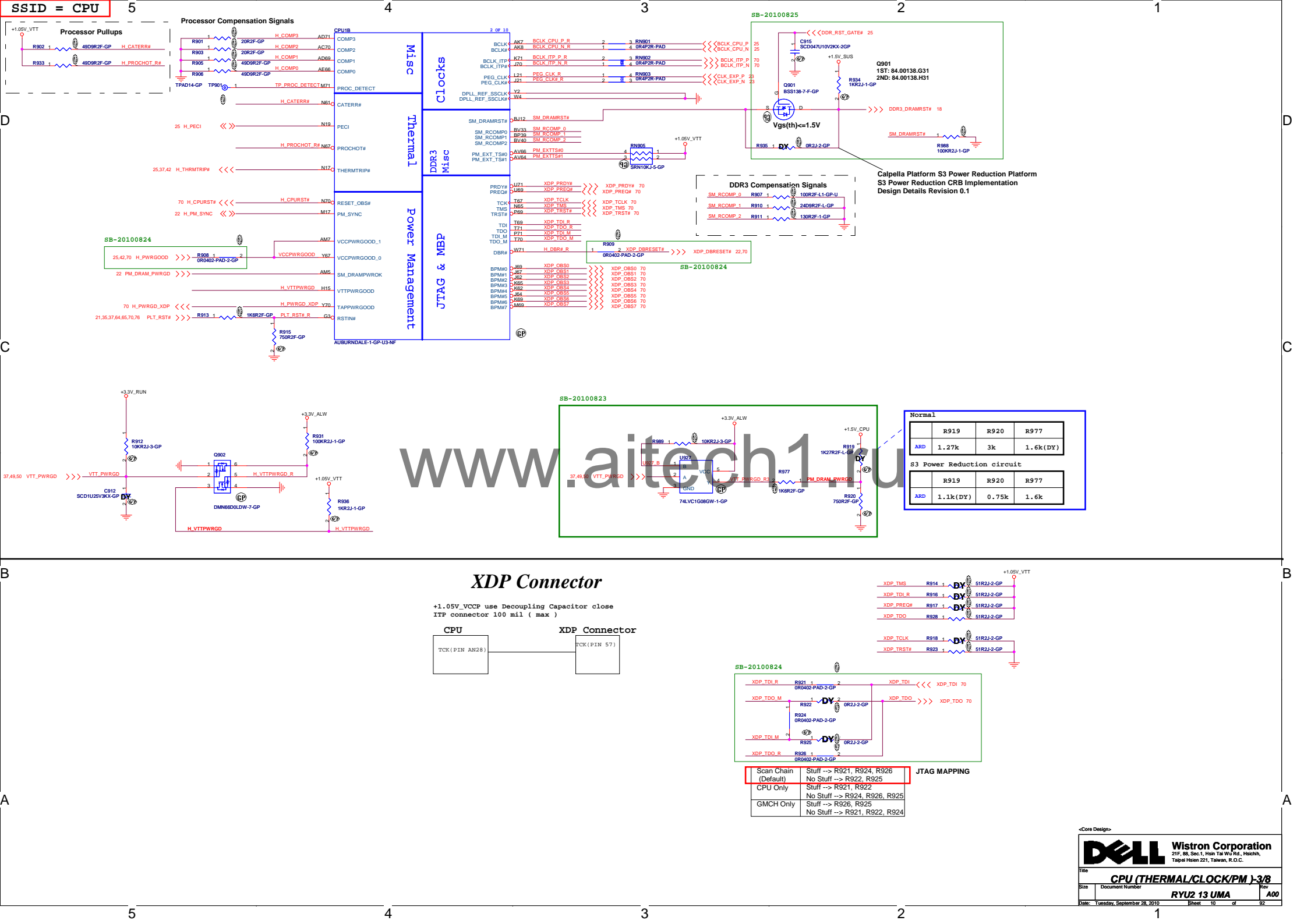
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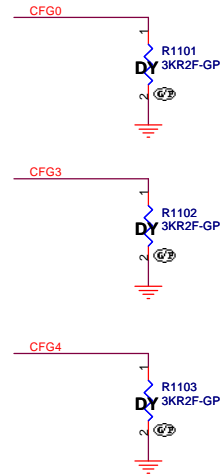
SSID = CPU



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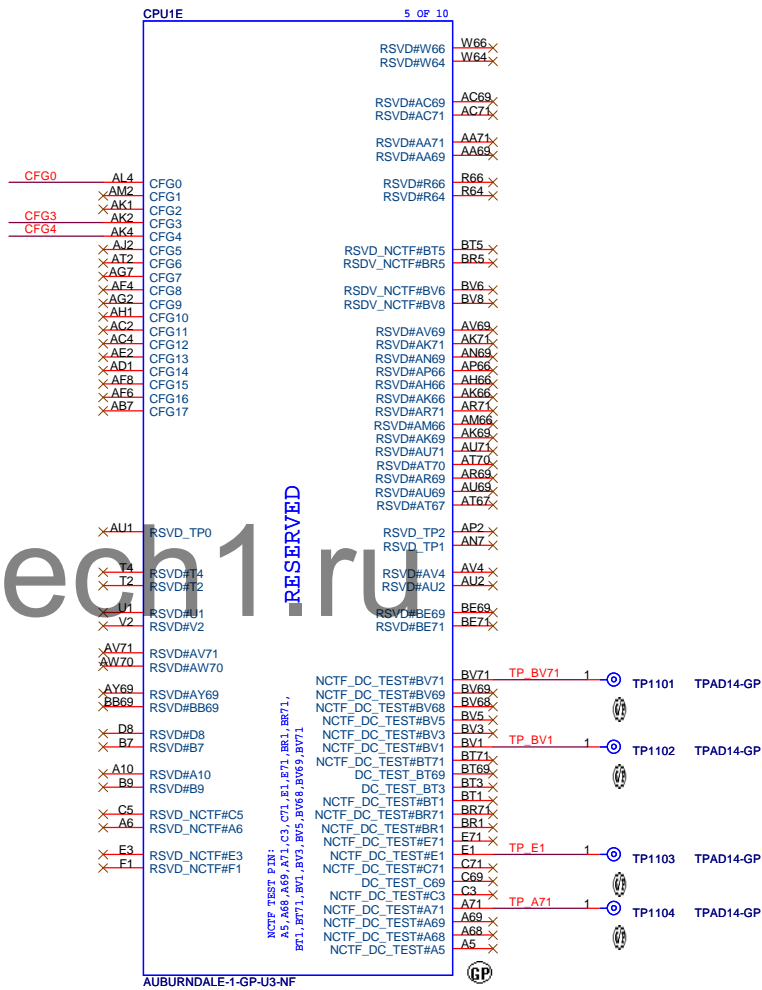
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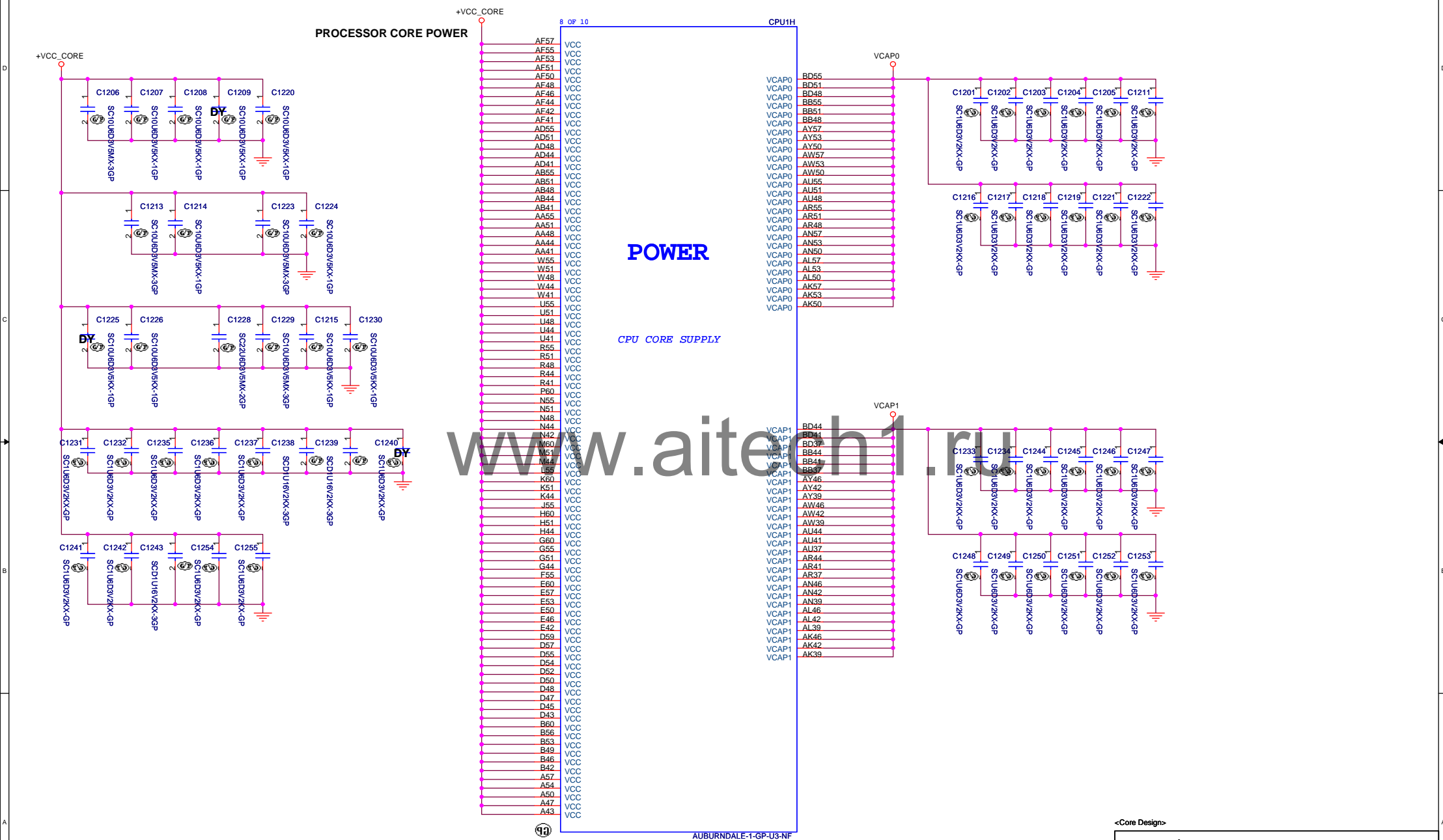
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Embedded DisplayPort Presence	
CFG4	1:Disabled - No Physical Display Port attached to Embedded DisplayPort 0:Enabled - An external DisplayPort device is connected to the Embedded DisplayPort



SSID = CPU



<Core Design>



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Title

CPU (VCC CORE)-6/8

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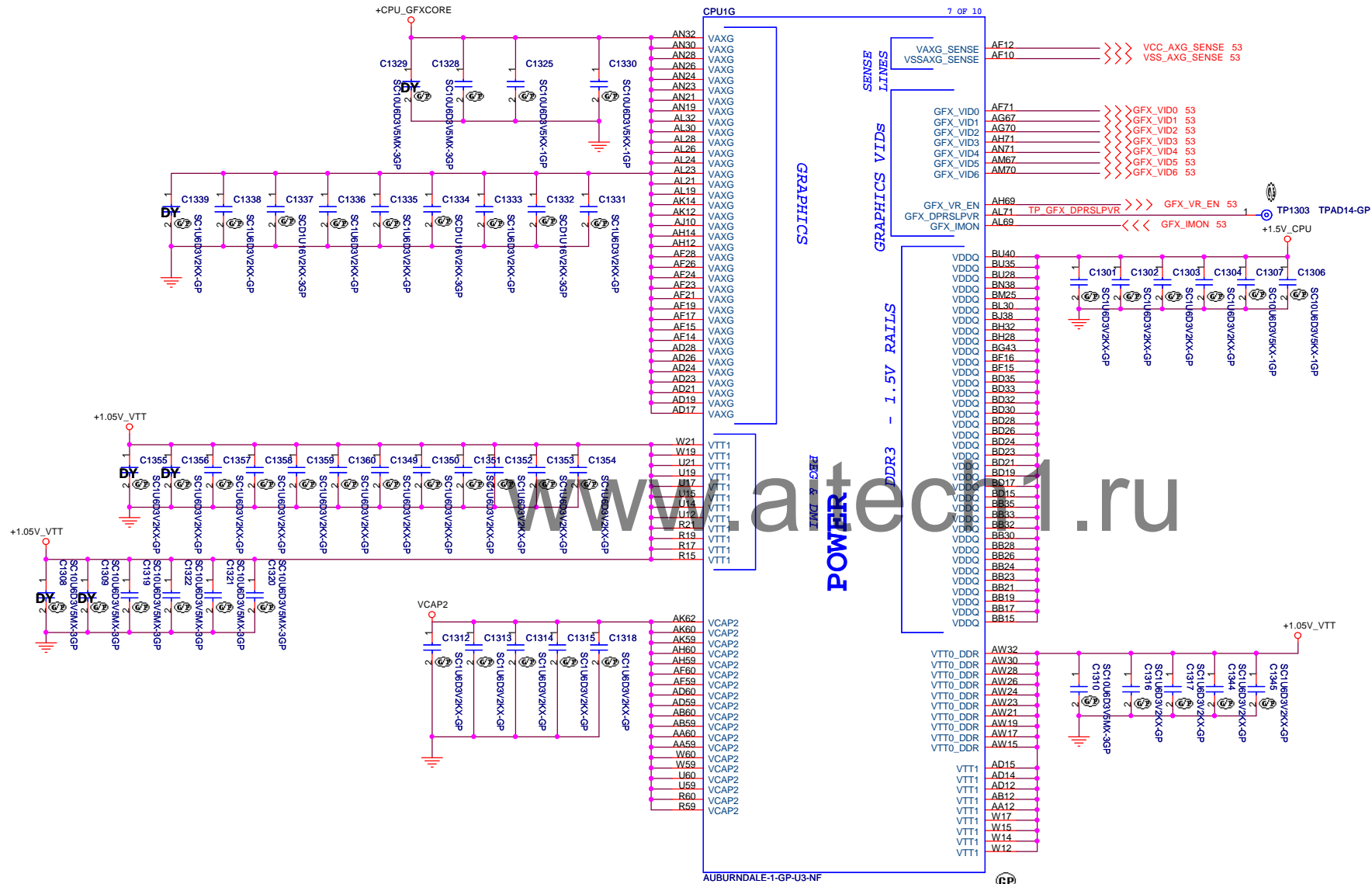
RYU2 13 UMA

Rev

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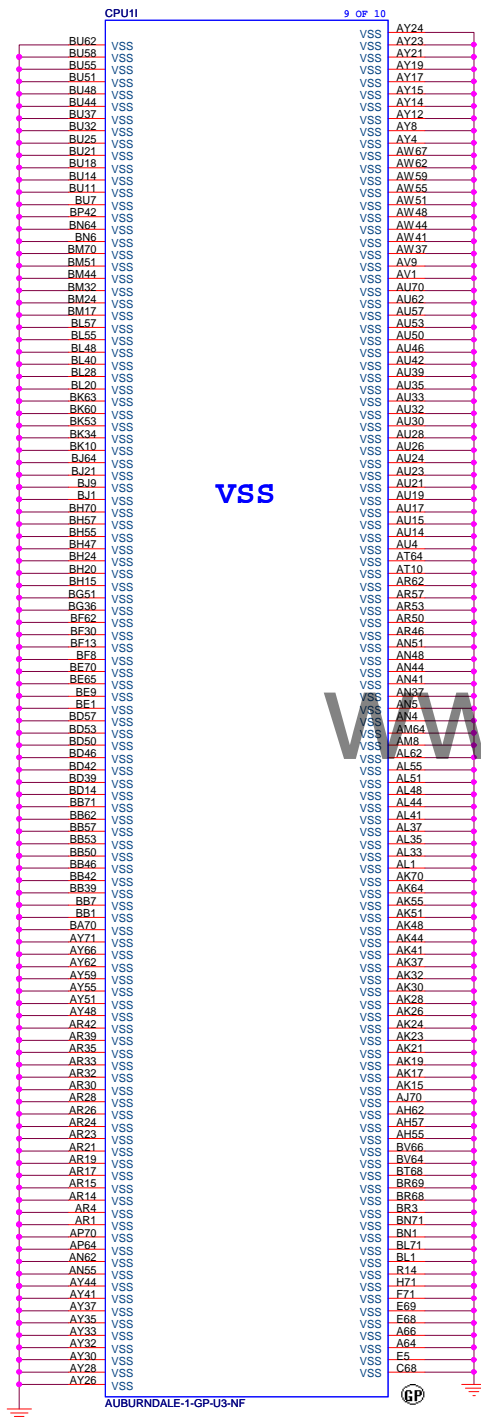
SSID = CPU



<Core Design>

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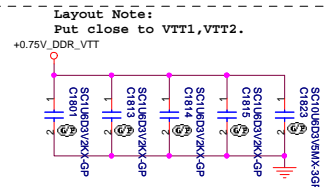
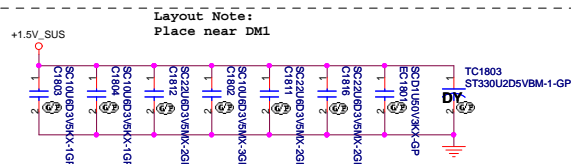
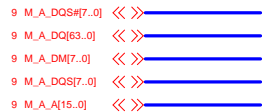


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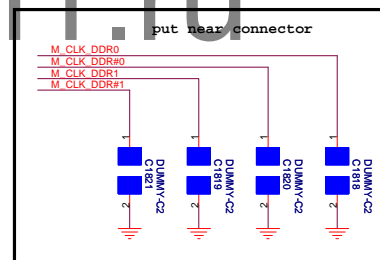
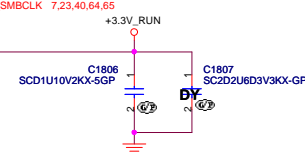
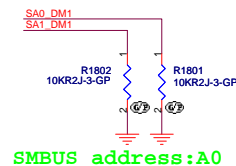
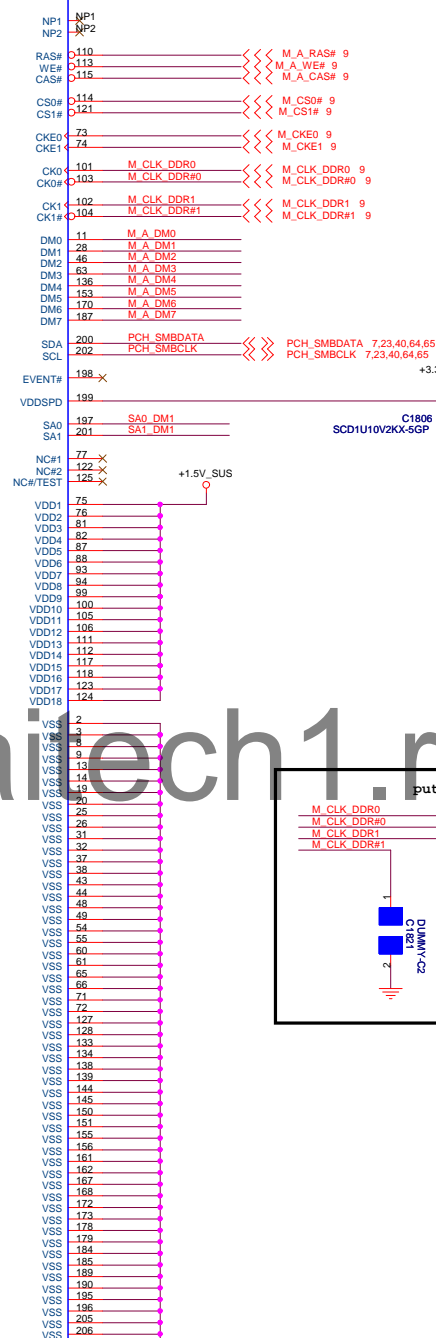
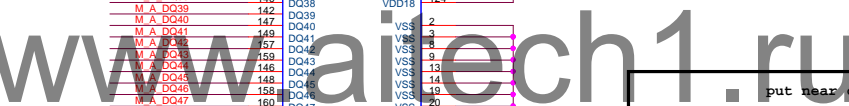
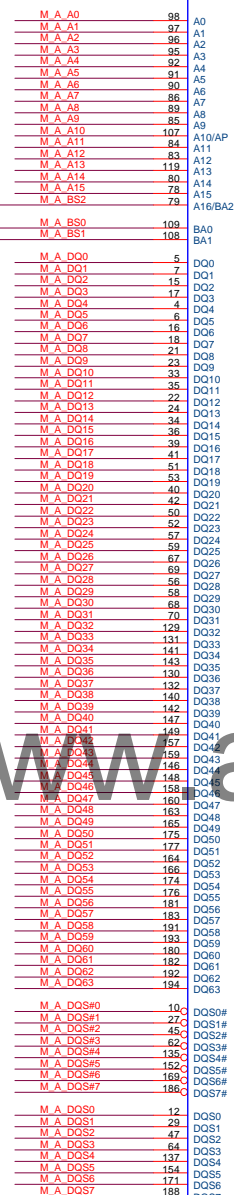
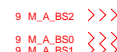
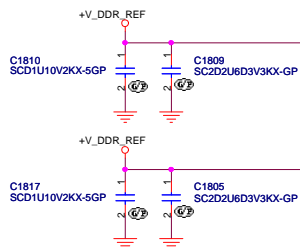
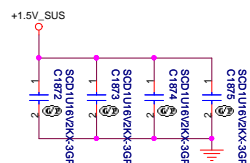


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SSID = MEMORY



Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9.pdf" document.

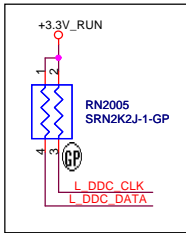


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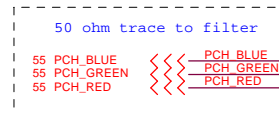
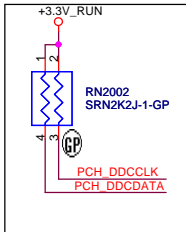
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SSID = PCH

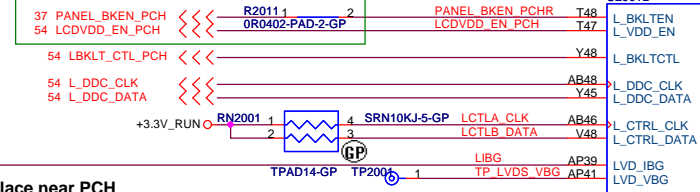
LVDS SMBUS
Close PCH



CRT SMBUS
Close PCH

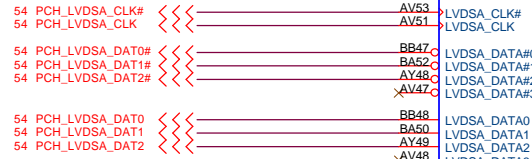


SB-20100824



Place near PCH

R2002
2K37R2F-GP



LVDSA_CLK#

LVDSA_CLK

LVDSA_DATA#0

LVDSA_DATA#1

LVDSA_DATA#2

LVDSA_DATA#3

LVDSA_DATA0

LVDSA_DATA1

LVDSA_DATA2

LVDSA_DATA3

LVDSB_CLK#

LVDSB_CLK

LVDSB_DATA#0

LVDSB_DATA#1

LVDSB_DATA#2

LVDSB_DATA#3

LVDSB_DATA0

LVDSB_DATA1

LVDSB_DATA2

LVDSB_DATA3

CRT_BLUE

CRT_GREEN

CRT_RED

CRT_DDC_CLK

CRT_DDC_DATA

CRT_HSYNC

CRT_VSYNC

DAI_IREF

CRT_IRTN

IBEXPEAK-M-GP-NF

IBEXPEAK-M-GP-NF

IBEXPEAK-M-GP-NF

IBEXPEAK-M-GP-NF

IBEXPEAK-M-GP-NF

IBEXPEAK-M-GP-NF

IBEXPEAK-M-GP-NF

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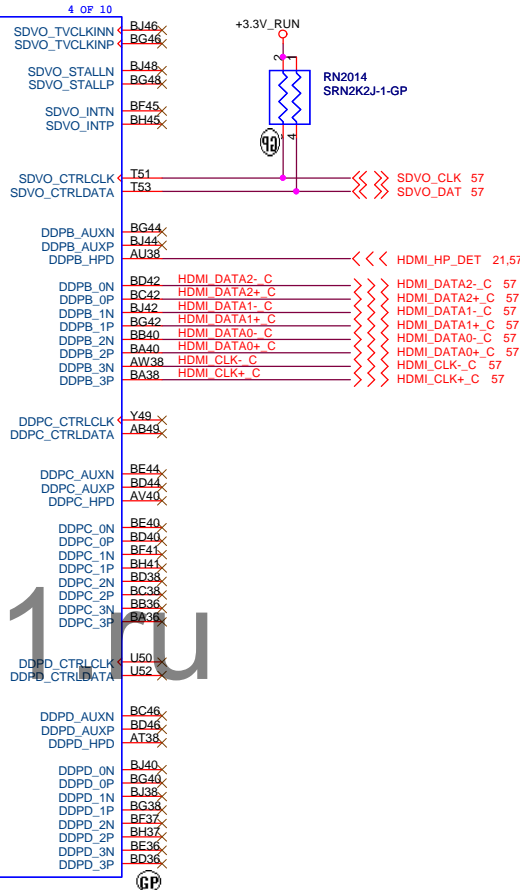
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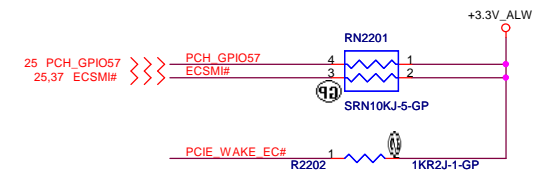
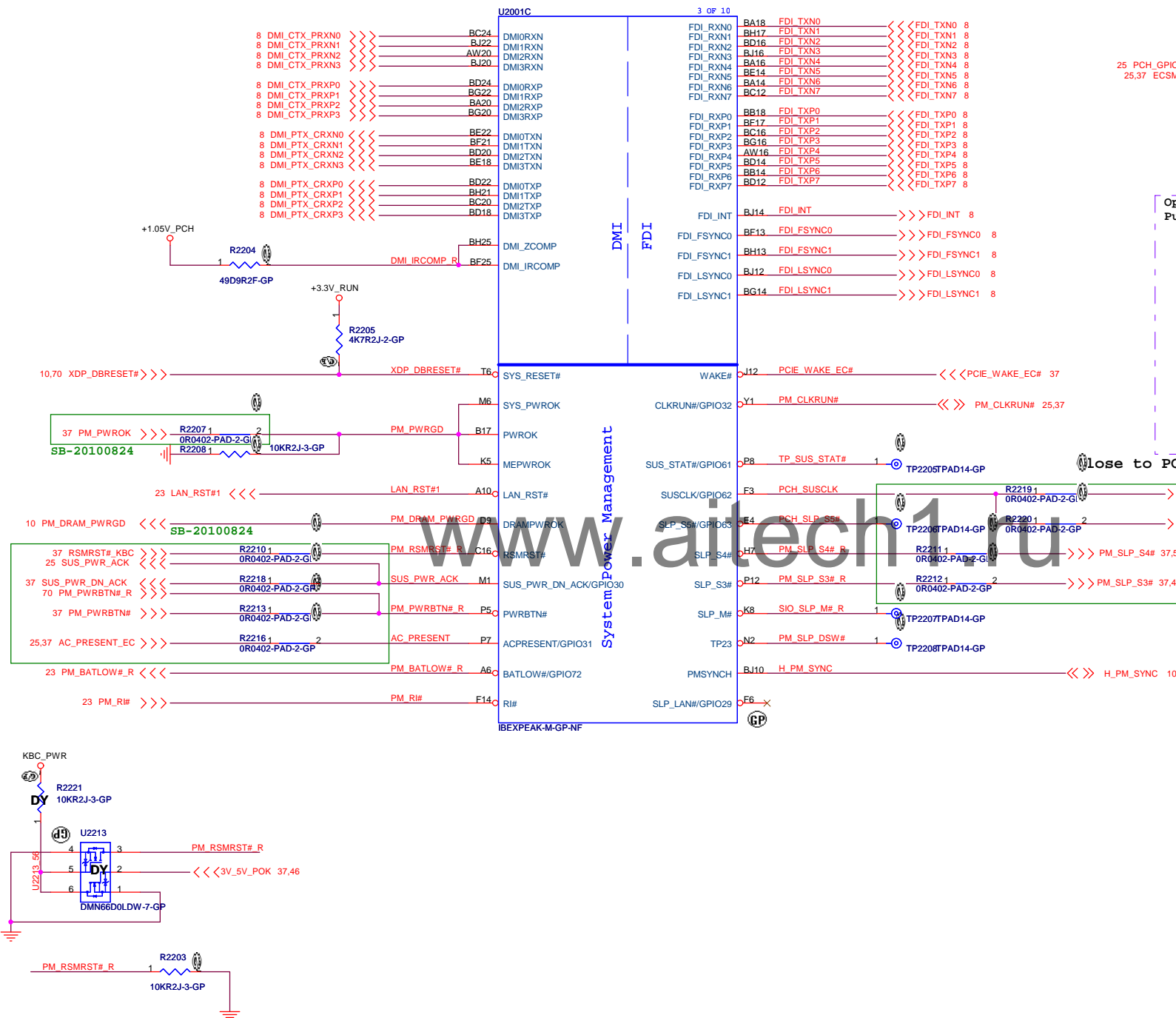
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Digital Display Interface

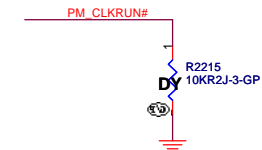


<Core Design>

SSID = PCH



Option to "Disable" clkrun.
Pulling it down will keep the clks running.



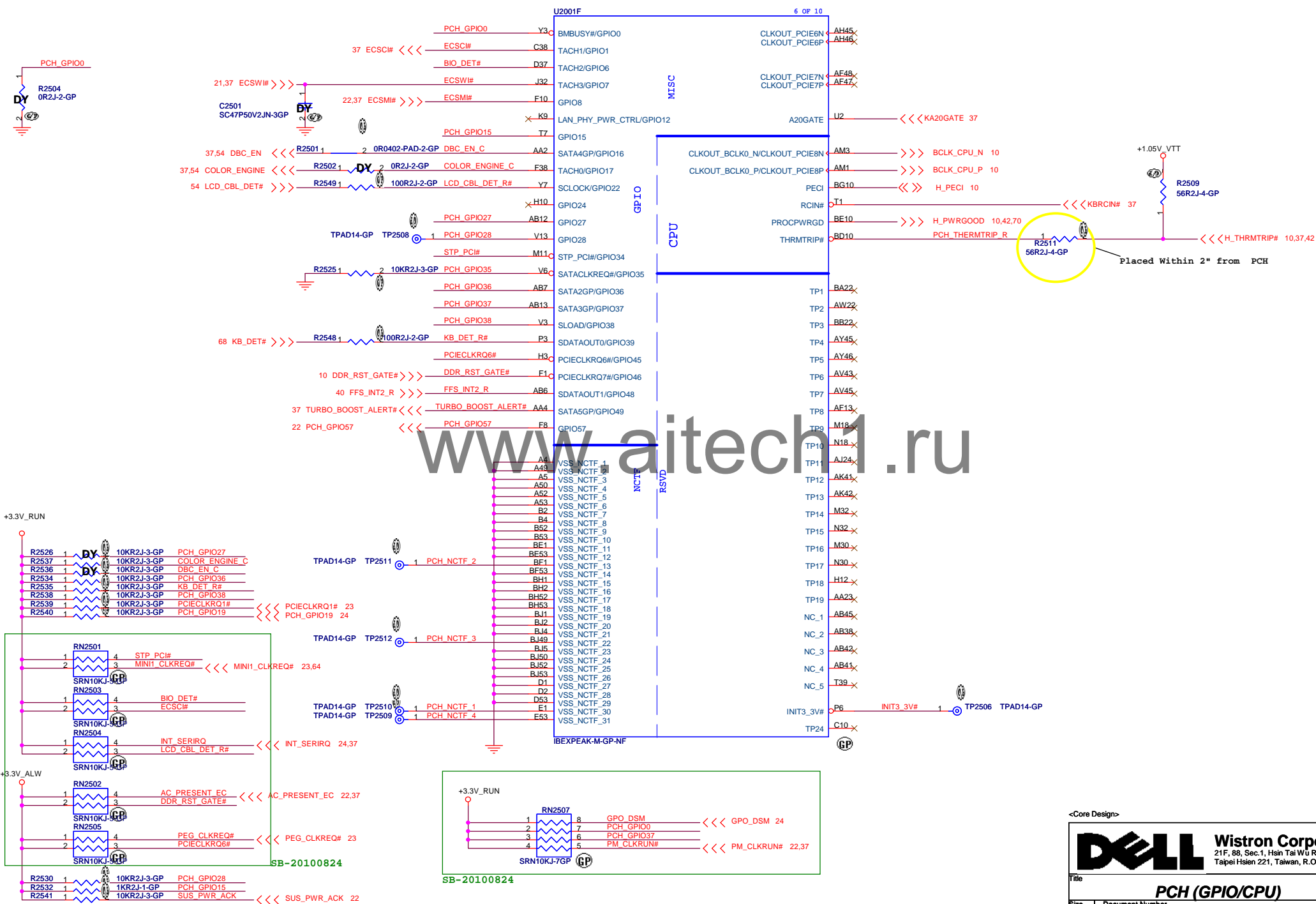
close to PCH

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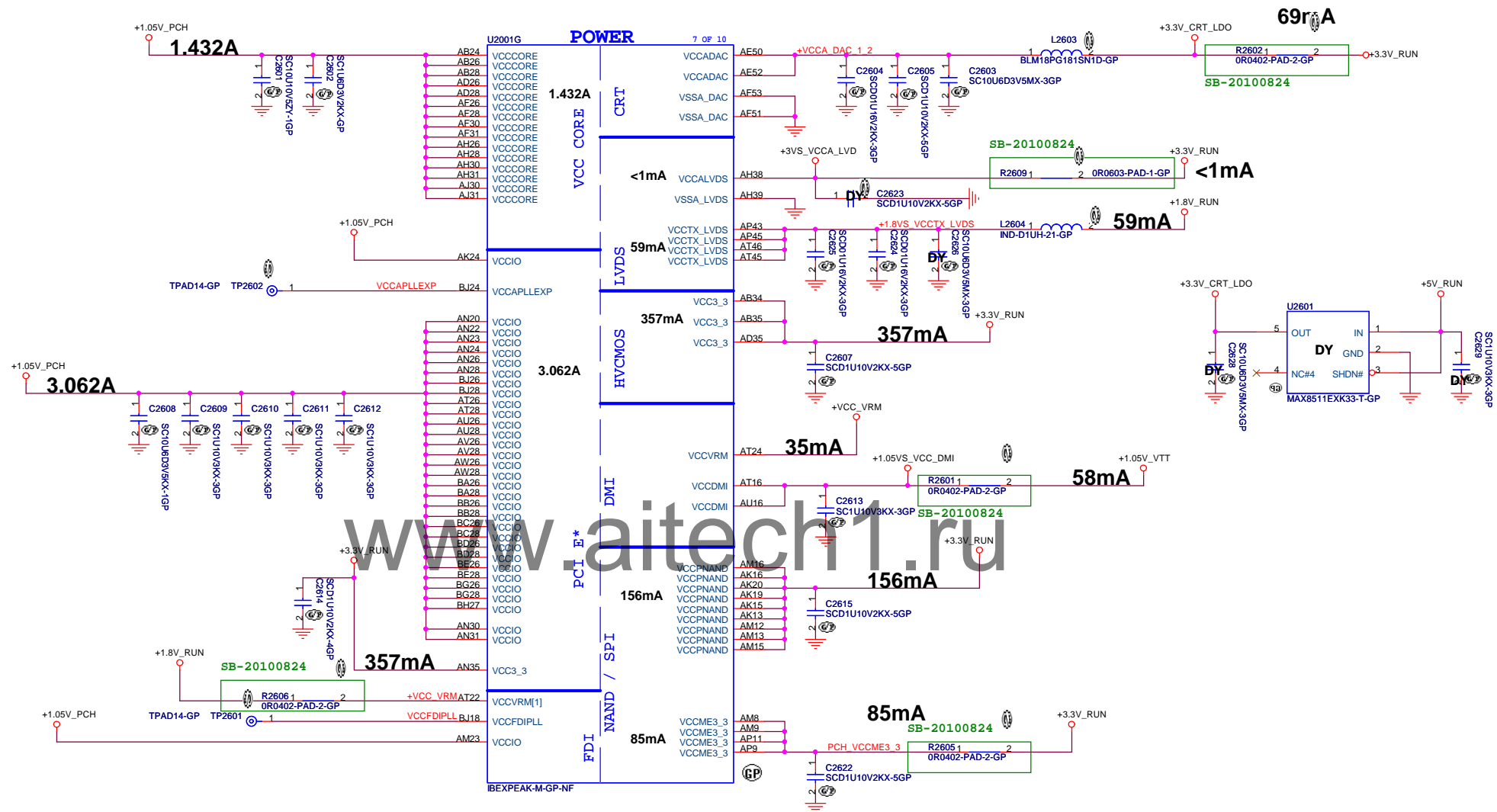
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Size: Document Number: **RYU2 13 UMA** Rev: **A00**
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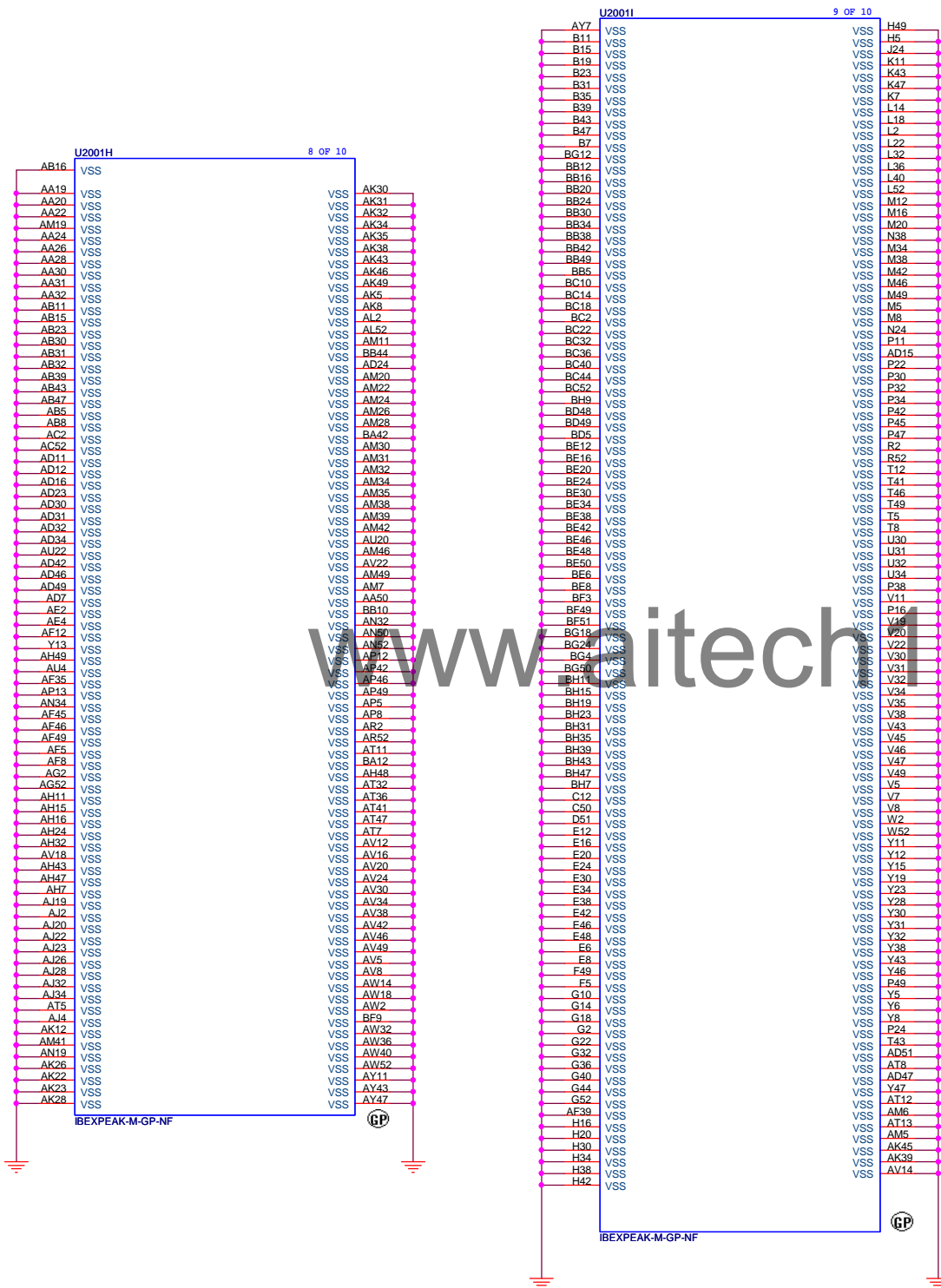
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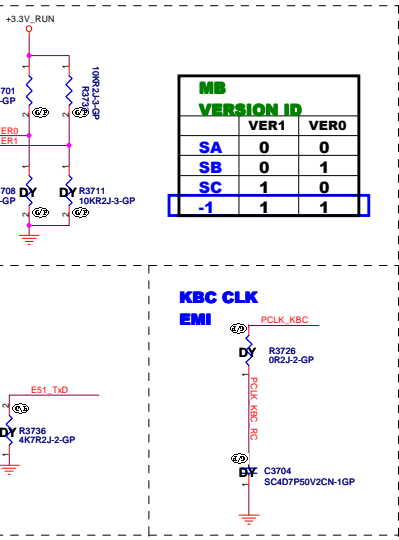
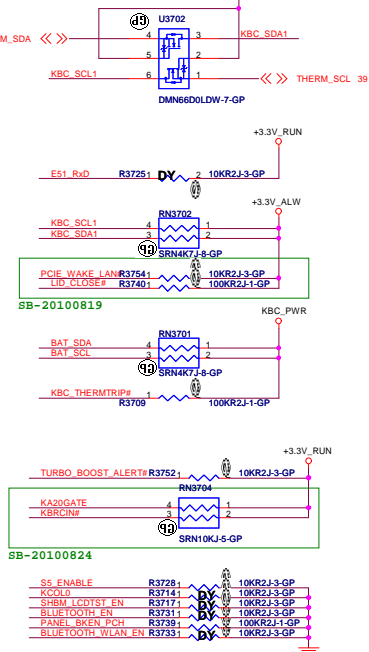
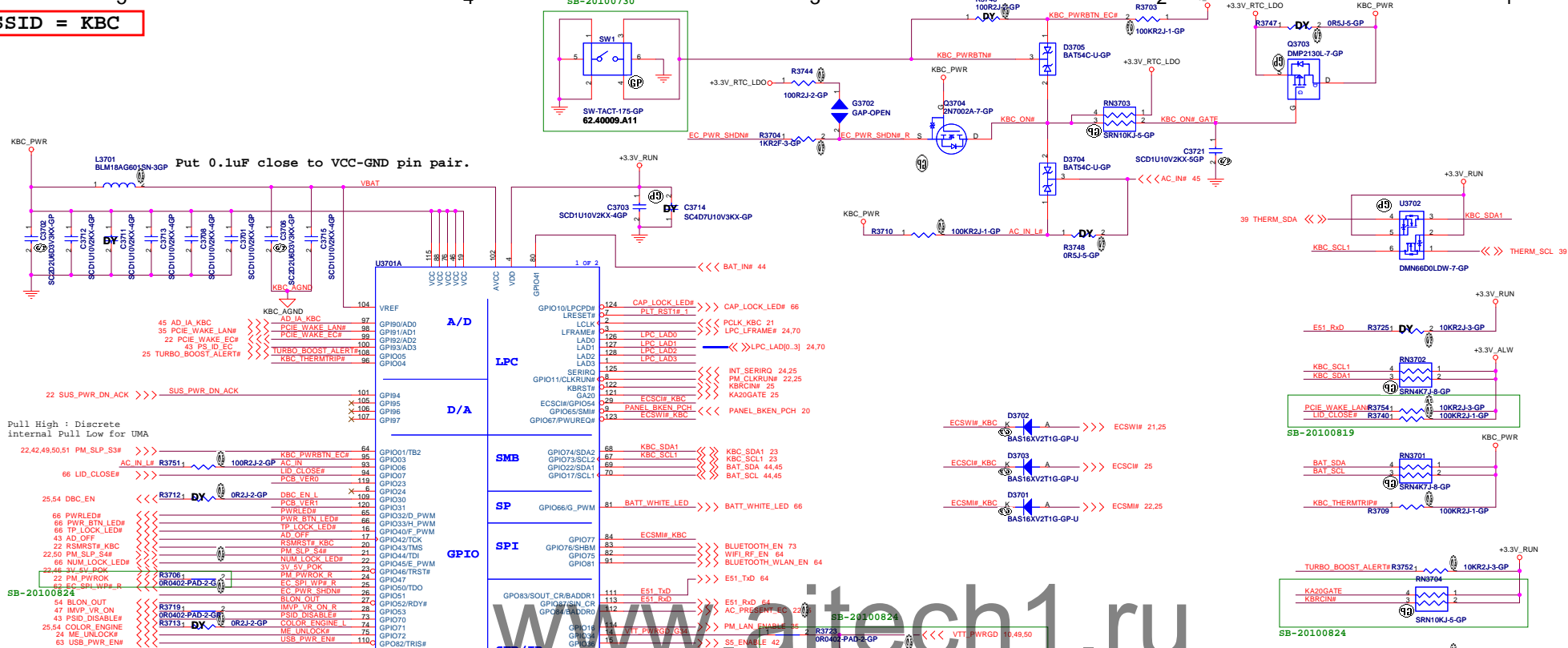
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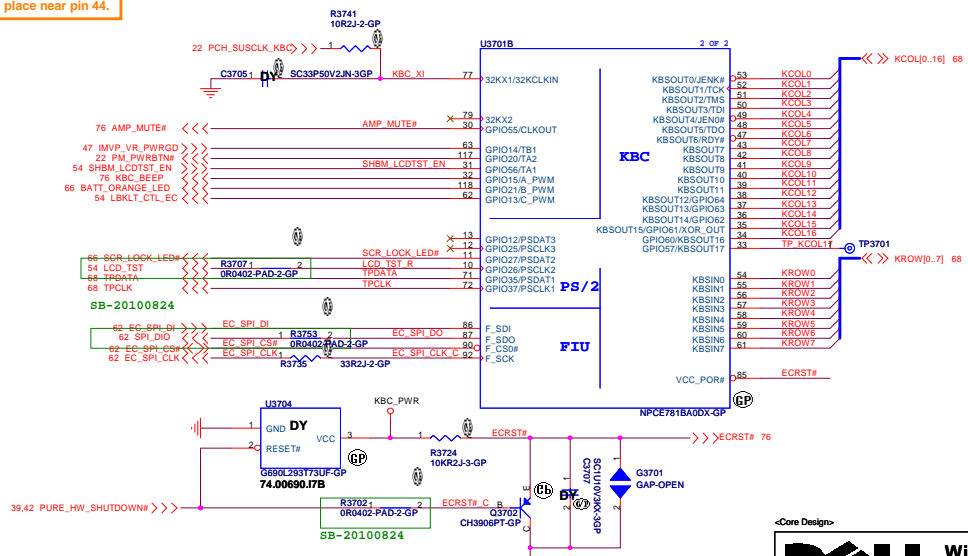
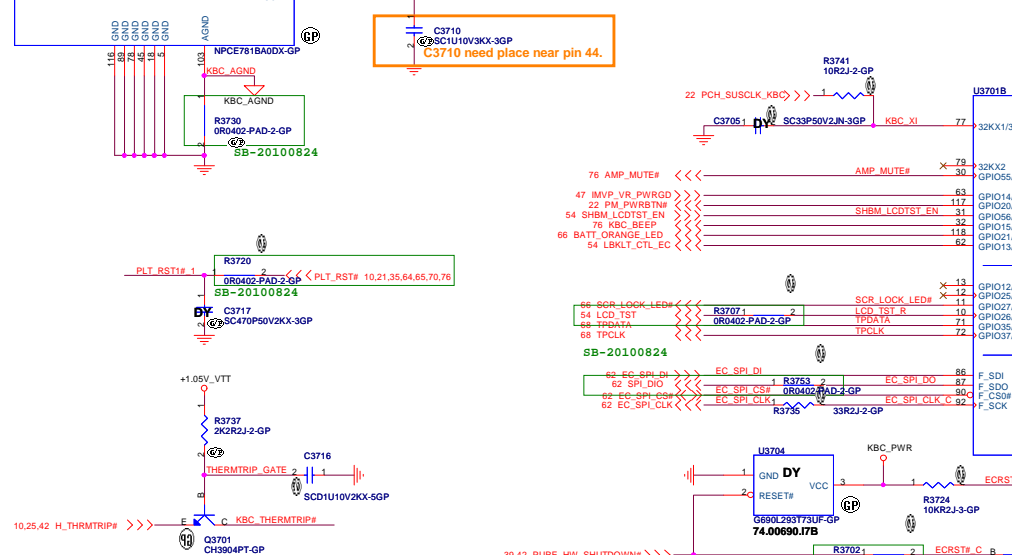
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SSID = KBC



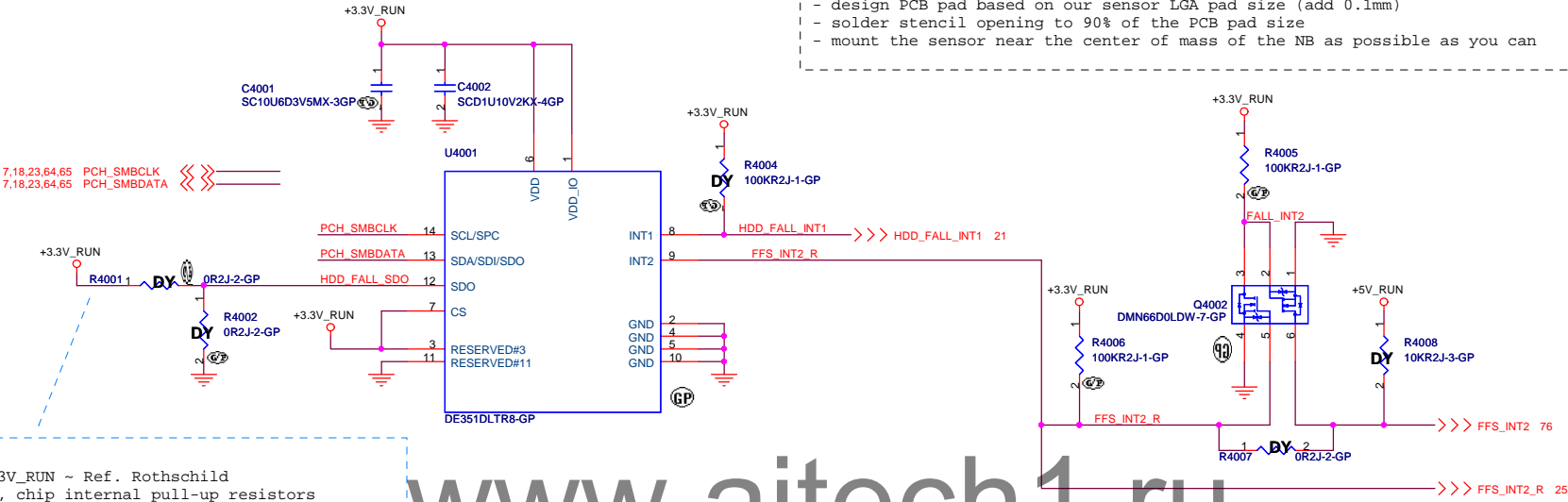
MB VERSION ID		
	VER1	VER0
SA	0	0
SB	0	1
SC	1	0
-1	1	1



Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422

(#1) Just pull +3.3V_RUN ~ Ref. Rothschild

(#2) FAE/ DY is ok, chip internal pull-up resistors

(#3) From spec, Slave Address(SAD) is 001110xb

Pull HIGH SAD is 0011101b

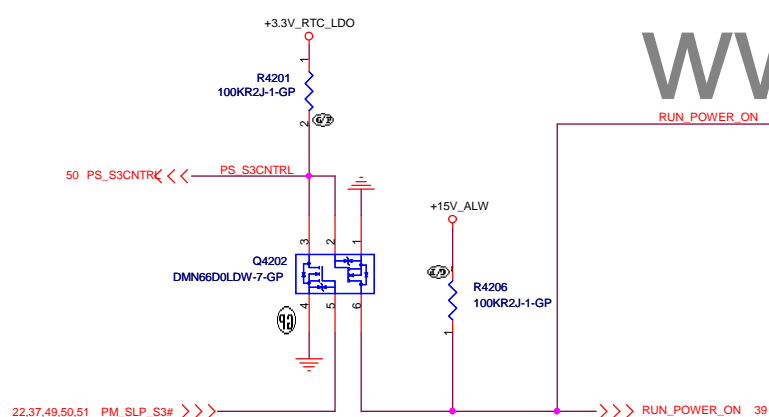
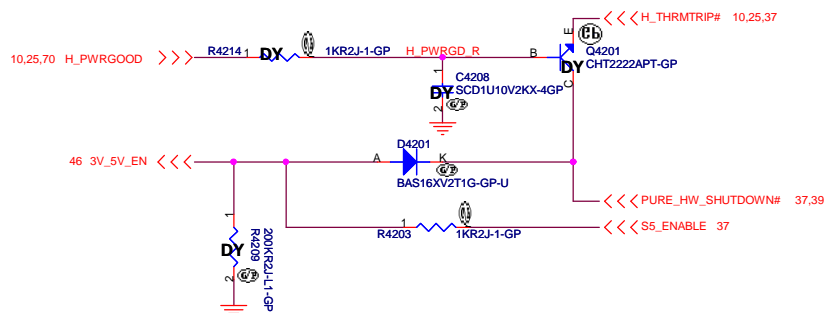
Pull GND SAD is 0011100b

Note

(1) Keep all signals are the same trace width. (included VDD, GND).

(2) No VIA under IC bottom.

SSID = Reset.Suspend

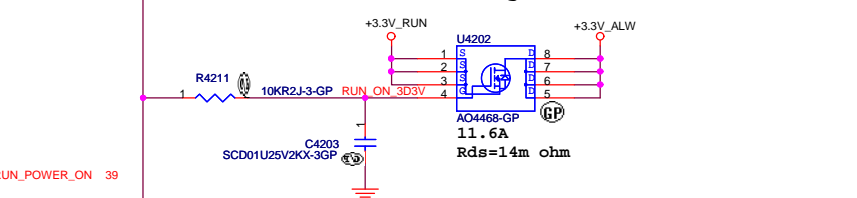


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Design current: 4246.6mA

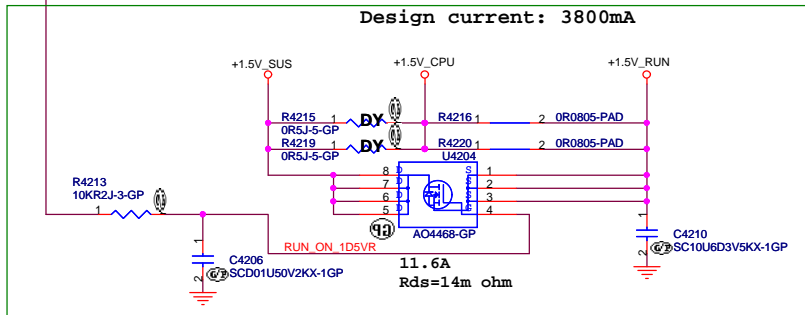


Design current: 6480.6mA



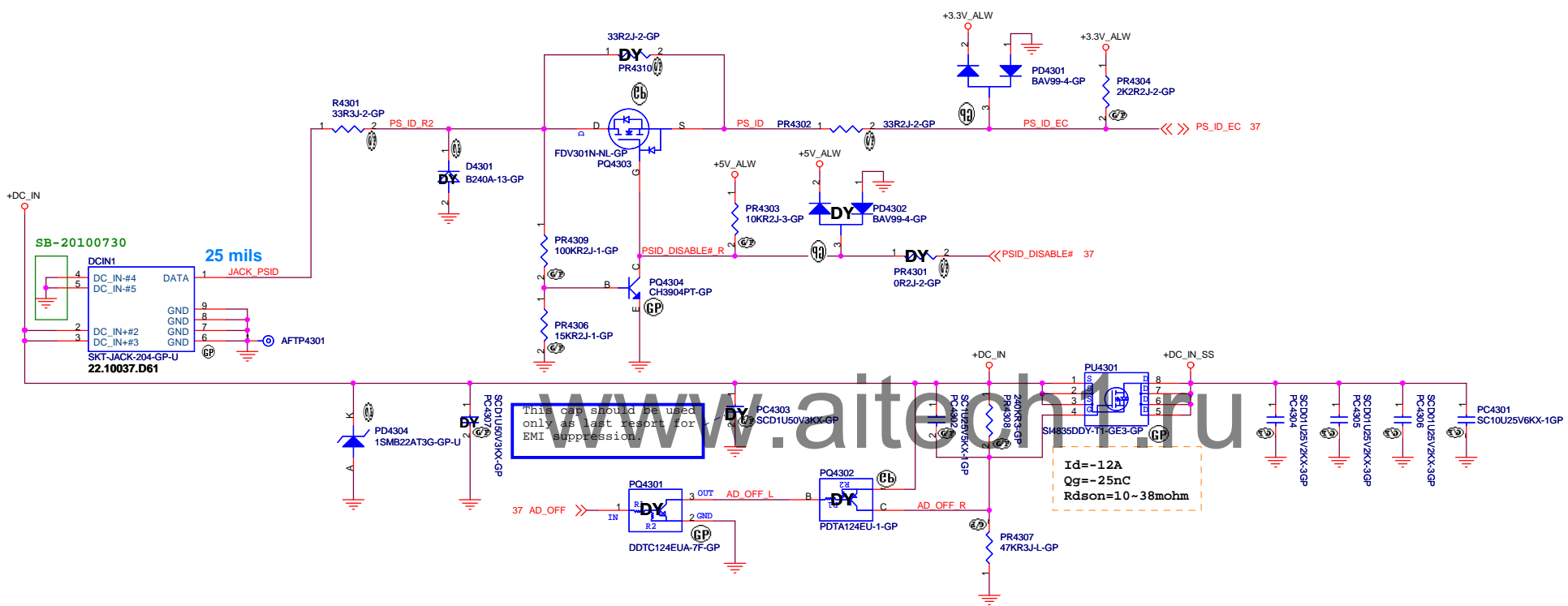
SB-20100823

Design current: 3800mA



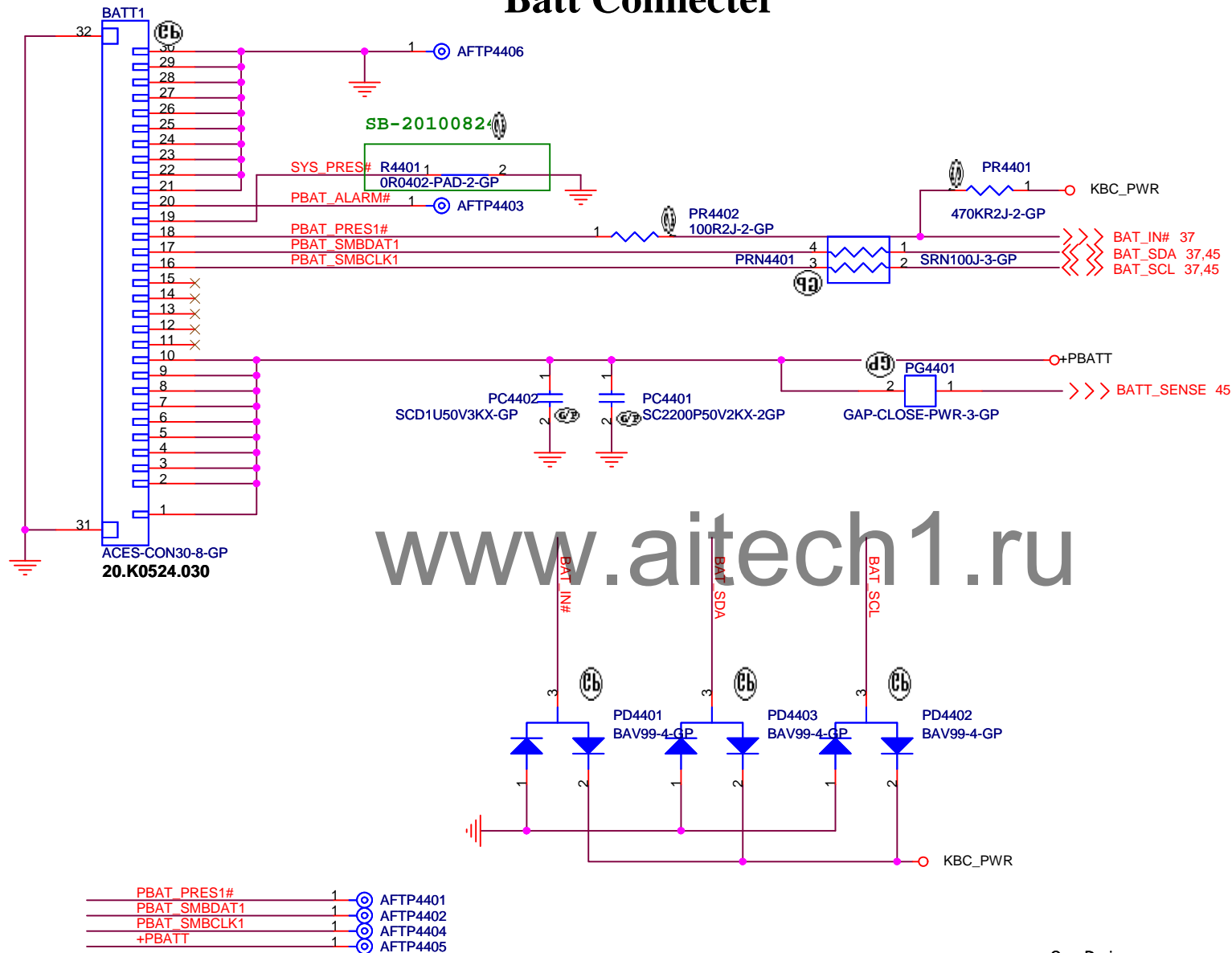
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SSID = DCIN



SSID = BATT

Batt Connector



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Batt Connector

Size
A4

Document Number

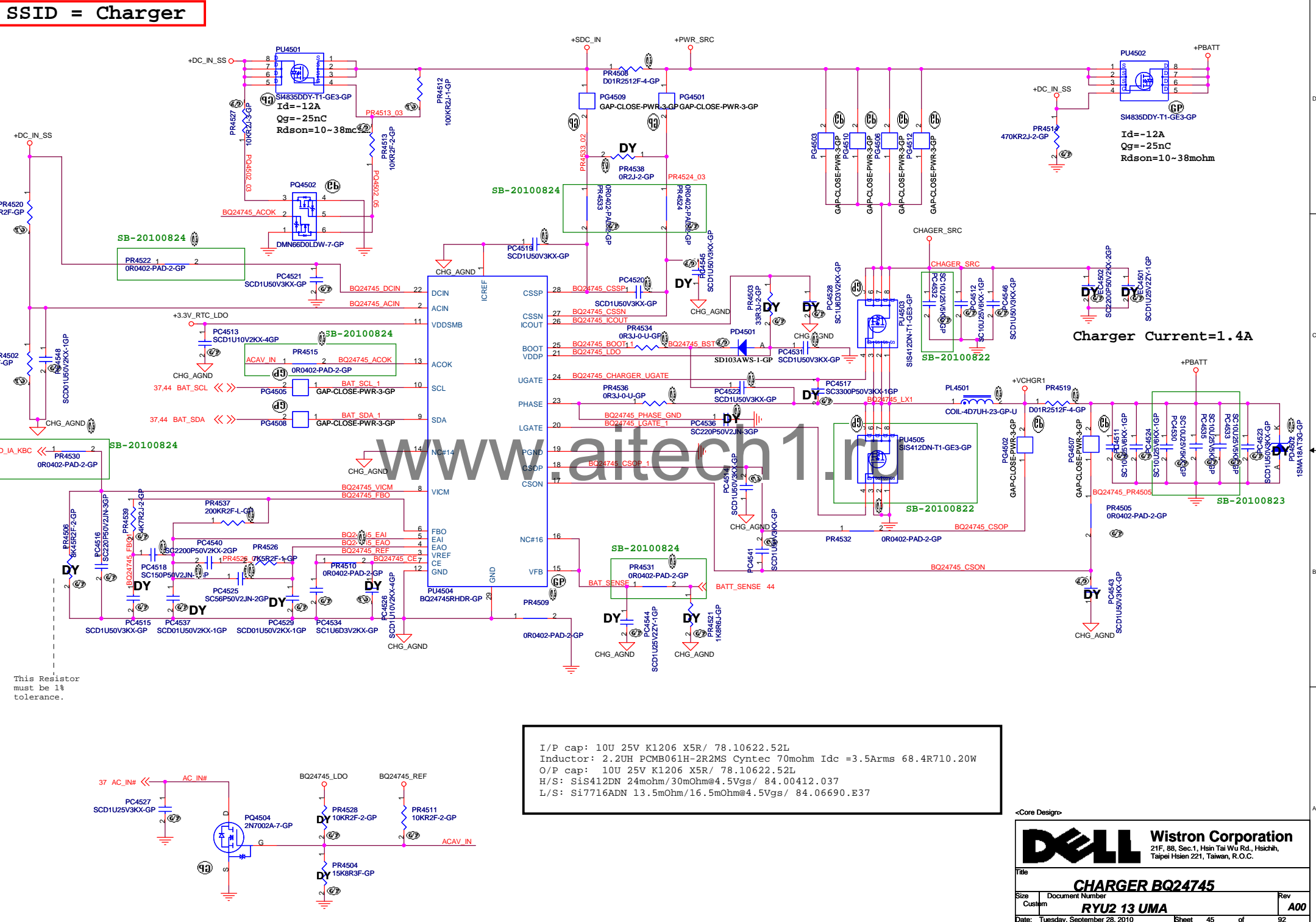
RYU2 13 UMA

Rev
A00

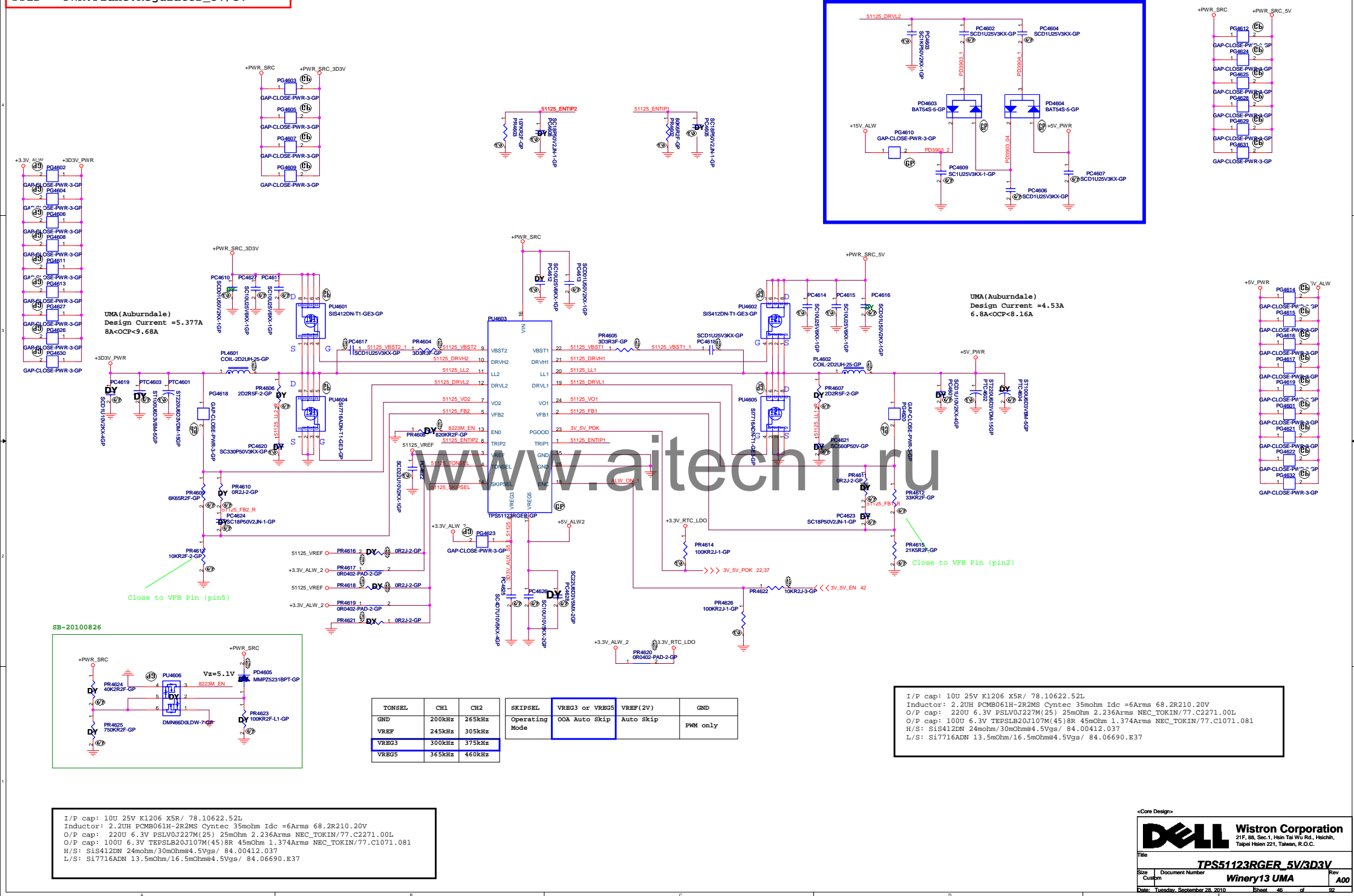
Date: Tuesday, September 28, 2010

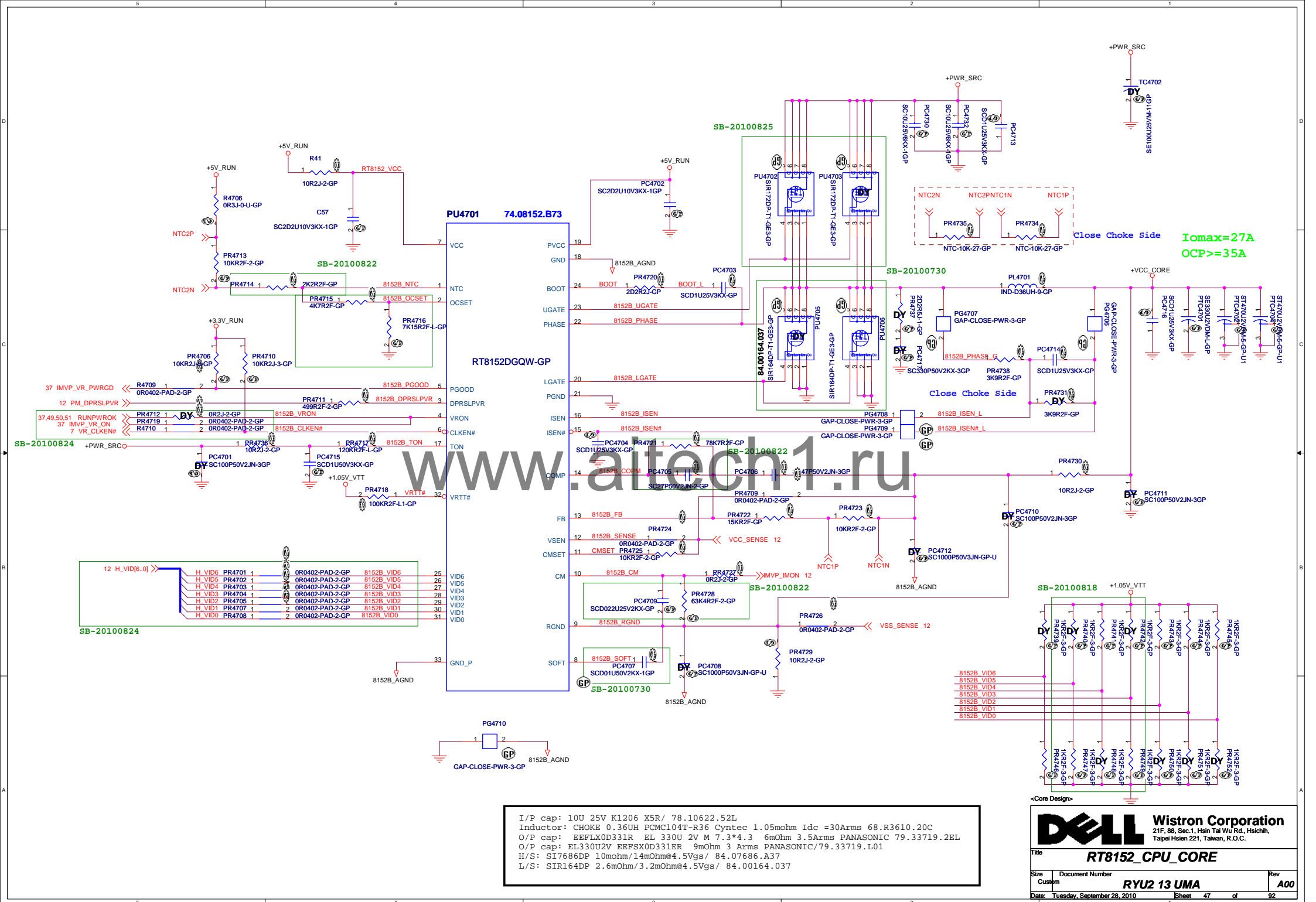
Sheet 44 of 92

SSID = Charger



SSID = PWR.Plane.Regulator_3V/5V





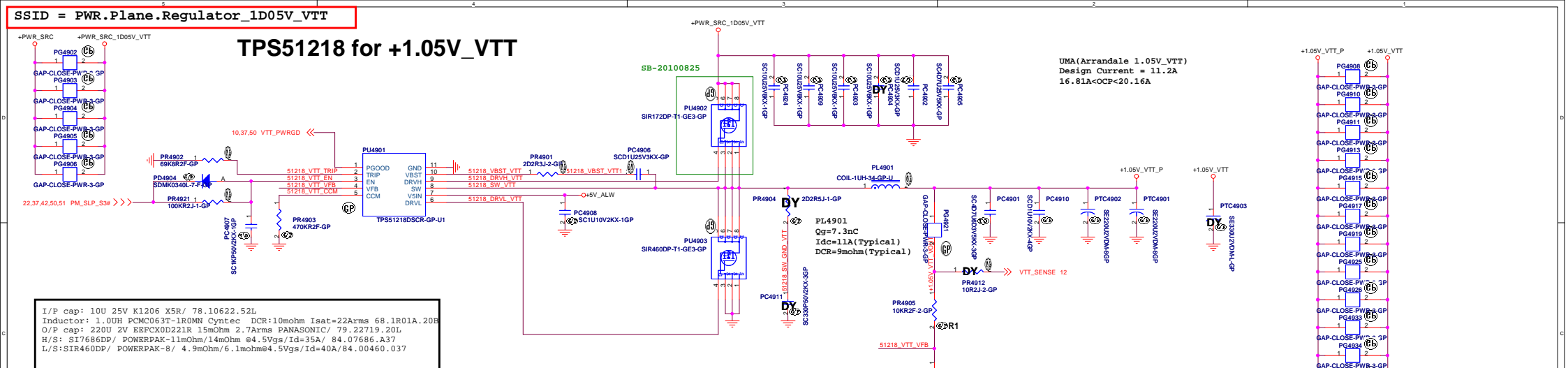
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

RT8152_CPU_CORE

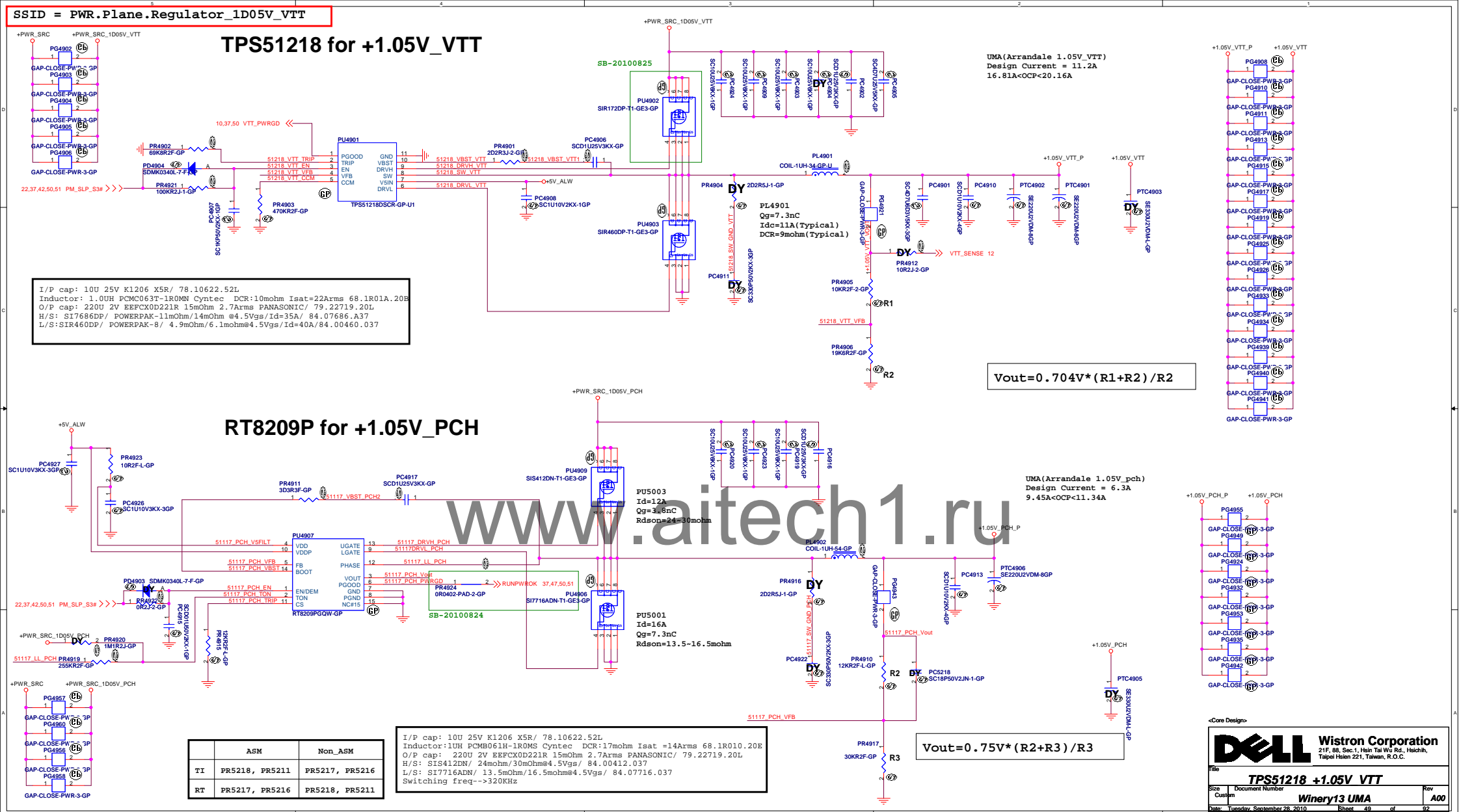
Size	Document Number	Rev
Custom	RYU2 13 UMA	A00

Date: Tuesday, September 28, 2010 Sheet 47 of 92

5	4	3	2	1
<div> <div>SSID = PWR.Plane.Regulator_1D05V VTT</div> <div>PWR_000_VREG_VTT</div> </div>				



5	4	3	2	1
SSID = PWR.Plane.Regulator_1D05V VTT			PWR_GPO_1D05V_VTT	



SSID = PWR.Regulator_ID05V_VTT

TPS51218 for +1.05V_VTT

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.0UH PCMC063T-1R0NM Cyntec DCR:10mohm Isat=22Arms 68.1R01A.20B
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-11mOhm/14mOhm @4.5Vgs/Id=35A/ 84.07686.A37
L/S: SIR460DP/ POWERPAK-8/ 4.9mohm/6.1mohm@4.5Vgs/Id=40A/84.00460.037

RT8209P for +1.05V_PCH

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1UH PCMB061H-1R0MS Cyntec DCR:17mohm Isat =14Arms 68.1R010.20B
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037
Switching freq-->320KHz

UMA(Arrandale 1.05V_VTT)
Design Current = 11.2A
16.81A<OCP<20.16A

UMA(Arrandale 1.05V_pch)
Design Current = 6.3A
9.45A<OCP<11.34A

Core Design

Dell Wistron Corporation
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei 10521, Taiwan, R.O.C.

TPS51218 +1.05V VTT

File: _____
Size: _____
Custm: _____
Date: Tuesday, September 28, 2010 Sheet: 49 of 92

	ASM	Non_ASM
TI	FR5218, FR5211	FR5217, FR5216
RT	FR5217, FR5216	FR5218, FR5211

Vout=0.704V*(R1+R2)/R2

Vout=0.75V*(R2+R3)/R3

SSID = PWR.Regulator_1D05V_VTT

TPS51218 for +1.05V_VTT

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.0UH PCMC063T-1R0NM Cyntec DCR:10mohm Isat=22Arms 68.1R01A.20B
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-11mOhm/14mOhm @4.5Vgs/Id=35A/ 84.07686.A37
L/S: SIR460DP/ POWERPAK-8/ 4.9mohm/6.1mohm@4.5Vgs/Id=40A/84.00460.037

RT8209P for +1.05V_PCH

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1UH PCMB061H-1R0MS Cyntec DCR:17mohm Isat =14Arms 68.1R010.20B
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037
Switching freq-->320KHz

UMA(Arrandale 1.05V_VTT)
Design Current = 11.2A
16.81A<OCP<20.16A

UMA(Arrandale 1.05V_pch)
Design Current = 6.3A
9.45A<OCP<11.34A

Core Design

TPS51218 +1.05V VTT

Winery13 UMA

Date: Tuesday, September 28, 2010 Sheet 49 of 92

SS1D = PWR.Regulator_ID05V_VTT

TPS51218 for +1.05V_VTT

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.0UH PCMC063T-1R0NM Cyntec DCR:10mohm Isat=22Arms 68.1R01A.20B
 O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
 H/S: SI7686DP/ POWERPAK-11mOhm/14mOhm @4.5Vgs/Id=35A/ 84.07686.A37
 L/S: SIR460DP/ POWERPAK-8/ 4.9mohm/6.1mohm@4.5Vgs/Id=40A/84.00460.037

UMA(Arrandale 1.05V_VTT)
 Design Current = 11.2A
 16.81A<OCP<20.16A

RT8209P for +1.05V_PCH

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1UH PCMB061H-1R0MS Cyntec DCR:17mohm Isat =14Arms 68.1R010.20B
 O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
 H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
 L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037
 Switching freq-->320KHz

UMA(Arrandale 1.05V_pch)
 Design Current = 6.3A
 9.45A<OCP<11.34A

Core Design

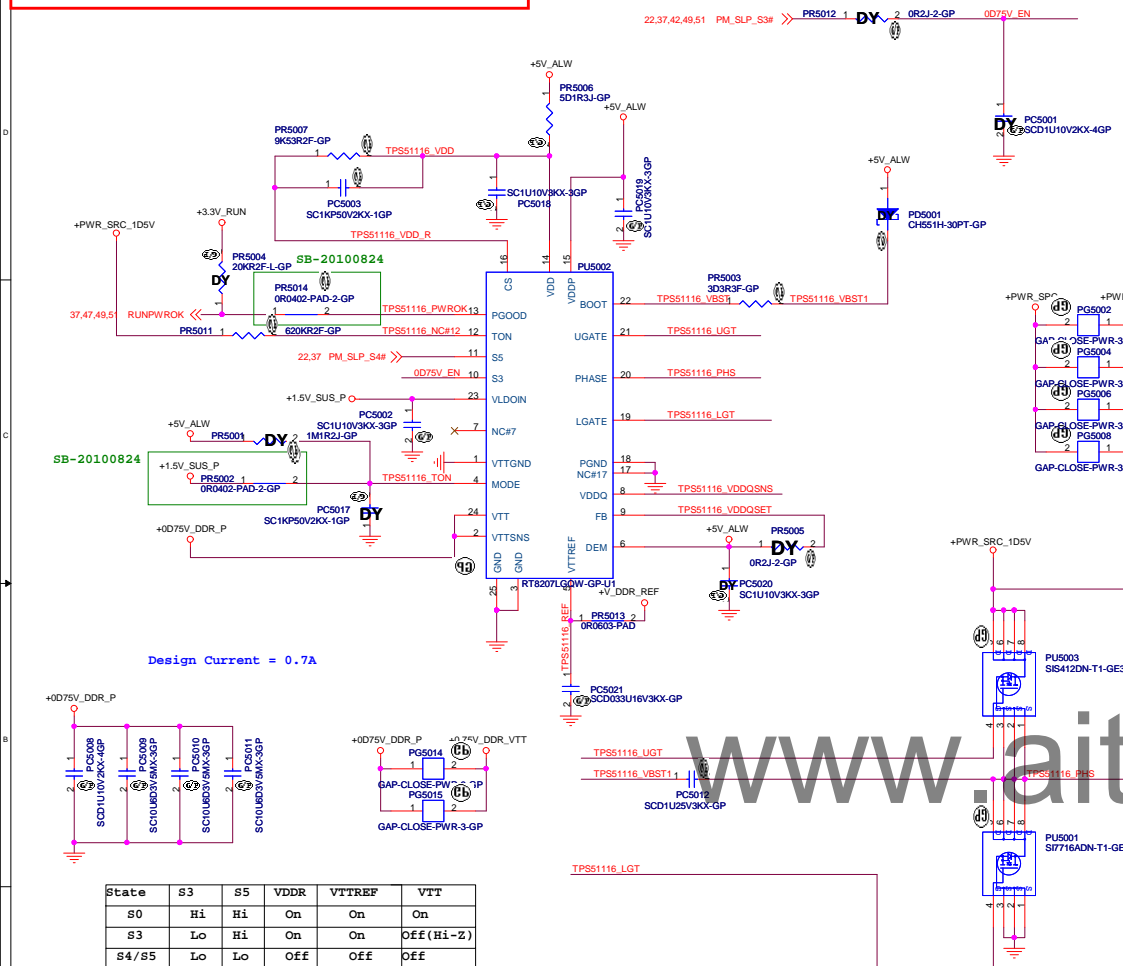
Dell Wistron Corporation
 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei 10521, Taiwan, R.O.C.

TPS51218 +1.05V VTT

File: _____
 Size: _____
 Date: Tuesday, September 28, 2010 10:48:49 AM

Rev: _____
 Winery13 UMA

```
SSID = PWR.Plane.Regulator_1p5v0p75v
```

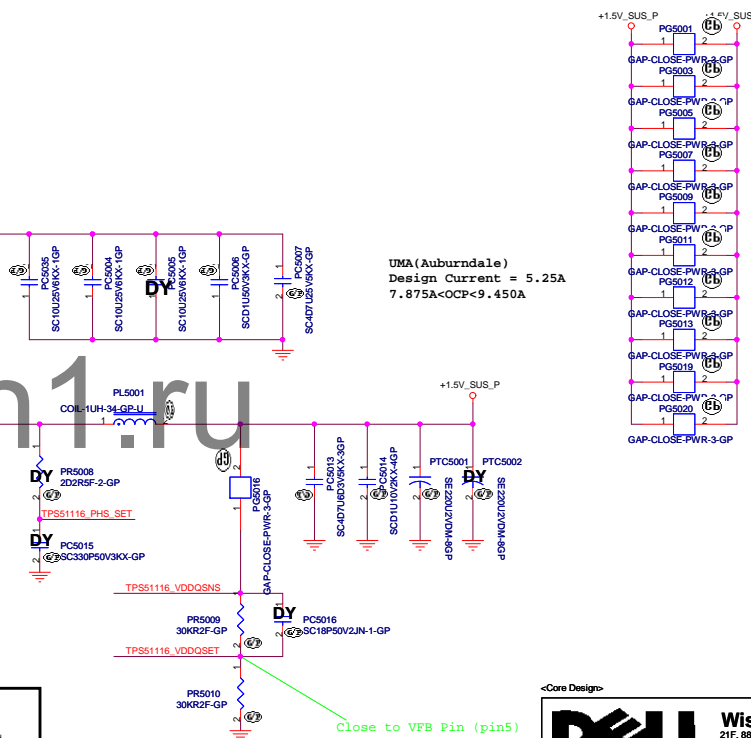
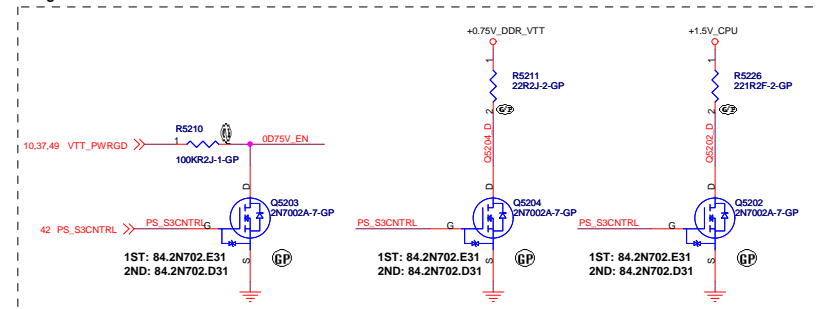


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VITREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

```
I/P cap: 10U 25V K206 X5R/ 78.10622.52L
Inductor: 1.0UH PCW0637C 180M 0.05% DCR:10mohm Isat=22Arms 68.1R01A.20B
O/P cap: O/P cap: 220U 2V EEFXCD0221R 15mohm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI8412DN/ 24mohm/30mohm@4.5Vgs/ 84.0412.037
L/S: SI7716ADN/ 13.5smohm/16.5mohm@4.5Vgs/ 84.07716.037
Switching freq-->400KHz
```

Calpella Platform S3 Power Reduction Platform S3 Power Reduction CRB Implementation Design Details



UMA(Auburndale)
Design Current = 5.25A
7.875A<OCP<9.450A

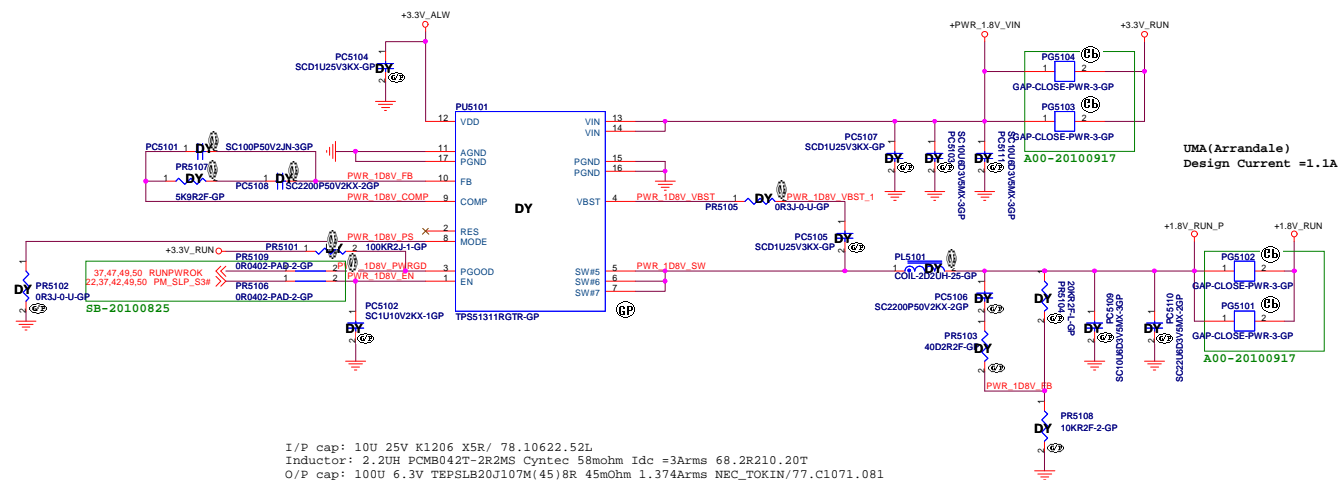
Close to VFB Pin (pin5)

<Core Design>



Title			
TPS51116 +1.5V SUS			
Size	Document Number		Rev
Custom	Winery13 UMA		A
Date:	Tuesday, September 28, 2010	Sheet 50 of	92

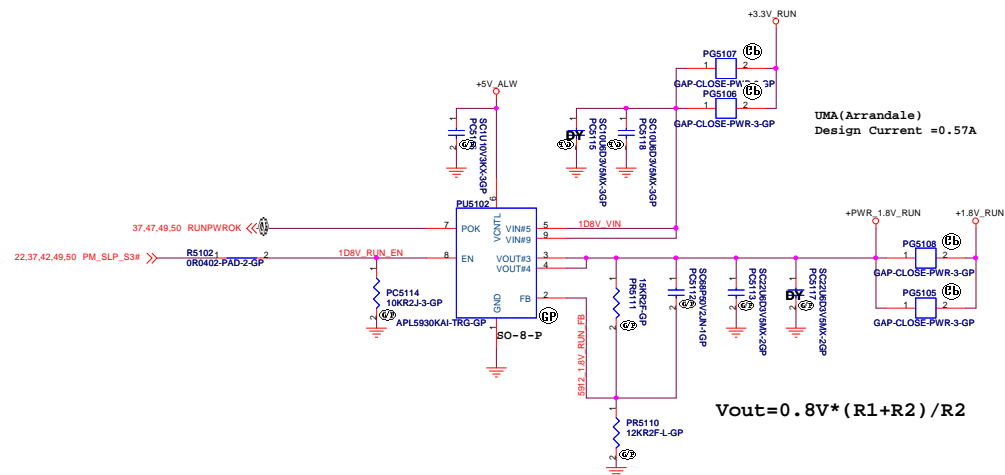
TPS51311RGTR for +1.8V_RUN



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH PCMB042T-2R2MS Cyntec 58mohm Idc =3Arms 68.2R210.20T
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081

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APL5930 for +1.8V_RUN



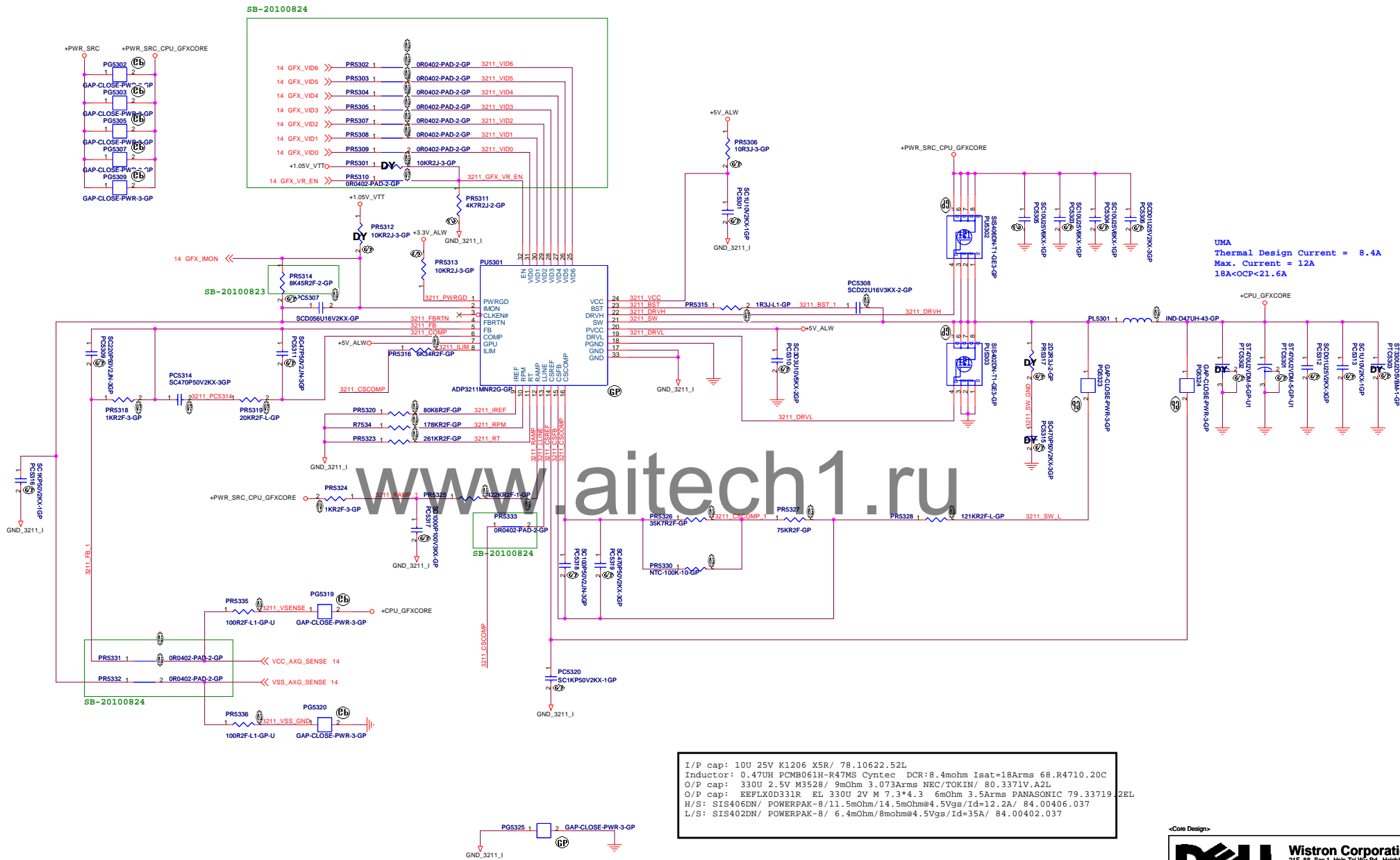
$$V_{out} = 0.8V * (R1 + R2) / R2$$

<Core Design>

DELL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

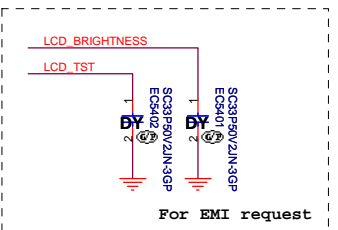
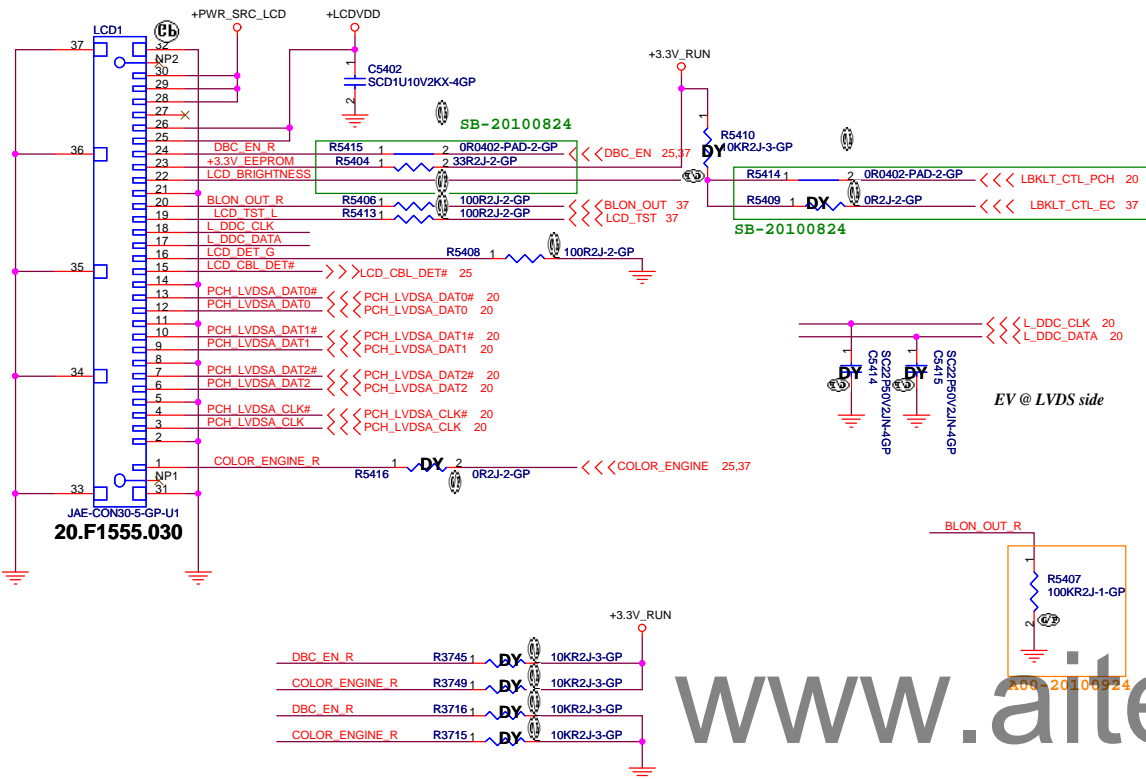
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Size		Document Number						Rev	
Custom		RYU2 13 UMA						A0	
Date: Tuesday, September 28, 2010				Sheet 51		of		92	



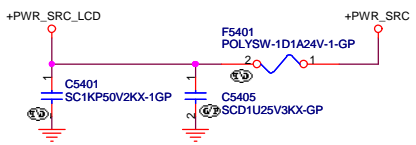
SSID = VIDEO

SSID = Inverter

LVDS CONNECTOR

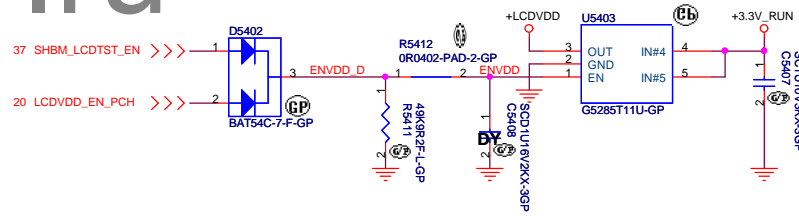


INVERTER POWER



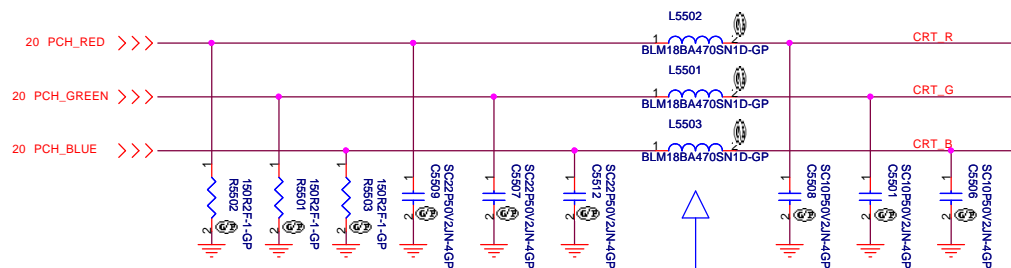
SSID = VIDEO

LCD POWER



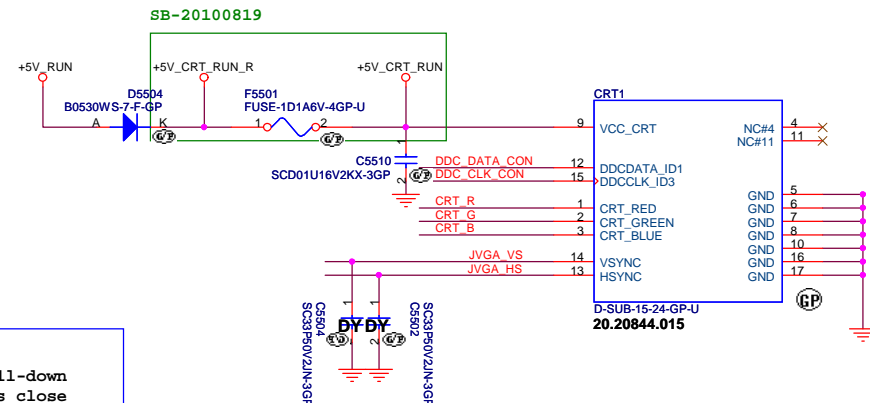
www.aitech1.ru

SSID = VIDEO



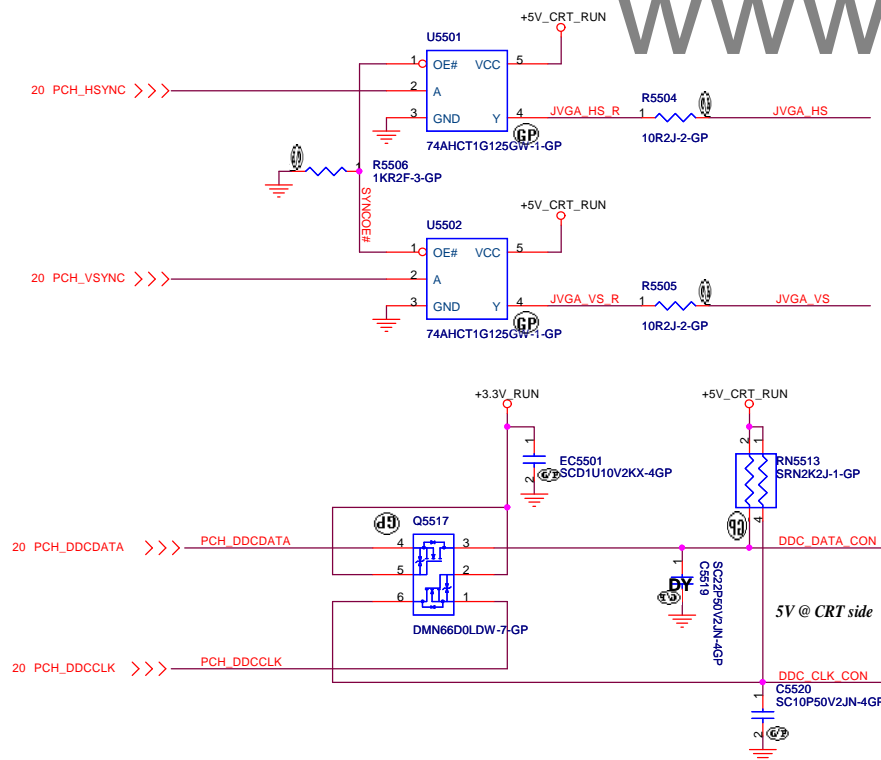
Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- *RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



Hsync & Vsync

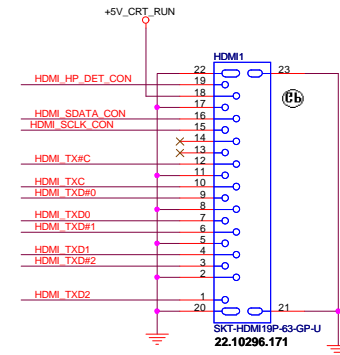
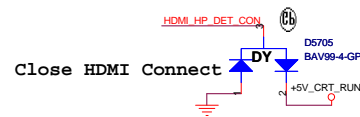
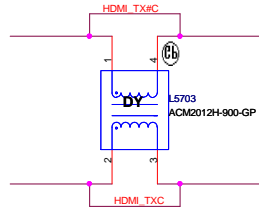
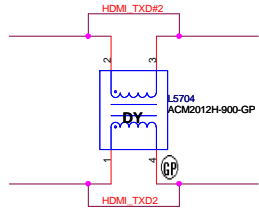
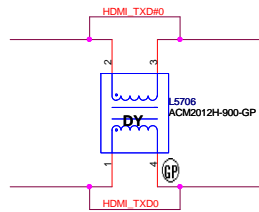
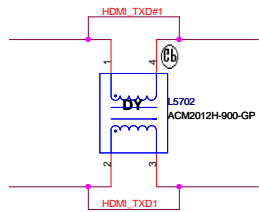
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<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CRT Connector	
Size	Document Number	Rev		
A3	RYU2 13 UMA	A00		
Date:	Tuesday, September 28, 2010	Sheet	55	of 92

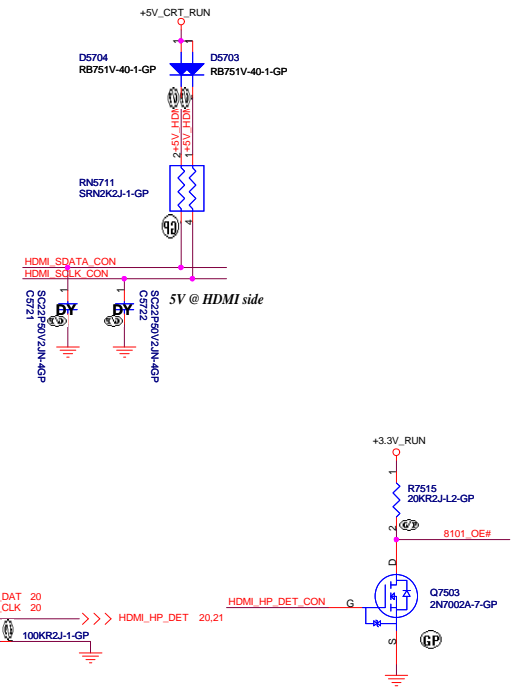
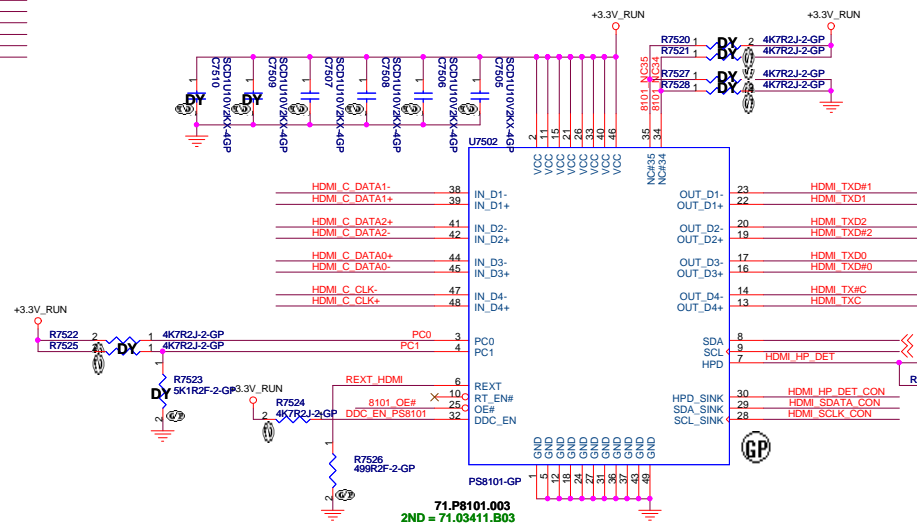


www.aitech1.ru

20	HDMI_DATA2+_C	C7561	1	SCD1U10V2KX-4GP	HDMI_C_DATA2+
20	HDMI_DATA2-_C	C7562	1	SCD1U10V2KX-4GP	HDMI_C_DATA2-
20	HDMI_DATA1+_C	C7563	1	SCD1U10V2KX-4GP	HDMI_C_DATA1+
20	HDMI_DATA1-_C	C7564	1	SCD1U10V2KX-4GP	HDMI_C_DATA1-
20	HDMI_DATA0+_C	C7565	1	SCD1U10V2KX-4GP	HDMI_C_DATA0+
20	HDMI_DATA0-_C	C7566	1	SCD1U10V2KX-4GP	HDMI_C_DATA0-
20	HDMI_CLK+_C	C7567	1	SCD1U10V2KX-4GP	HDMI_C_CLK+
20	HDMI_CLK-_C	C7568	1	SCD1U10V2KX-4GP	HDMI_C_CLK-

Close to PCH

UMA HDMI level shift circuit

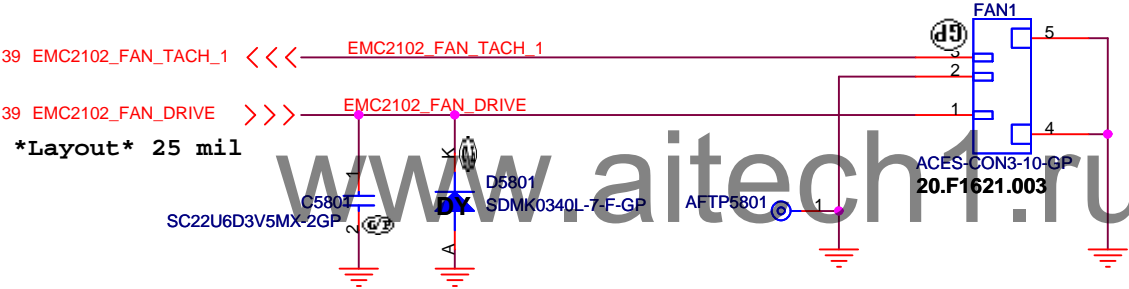


<Core Design>


SSID = Thermal

Fan Connector

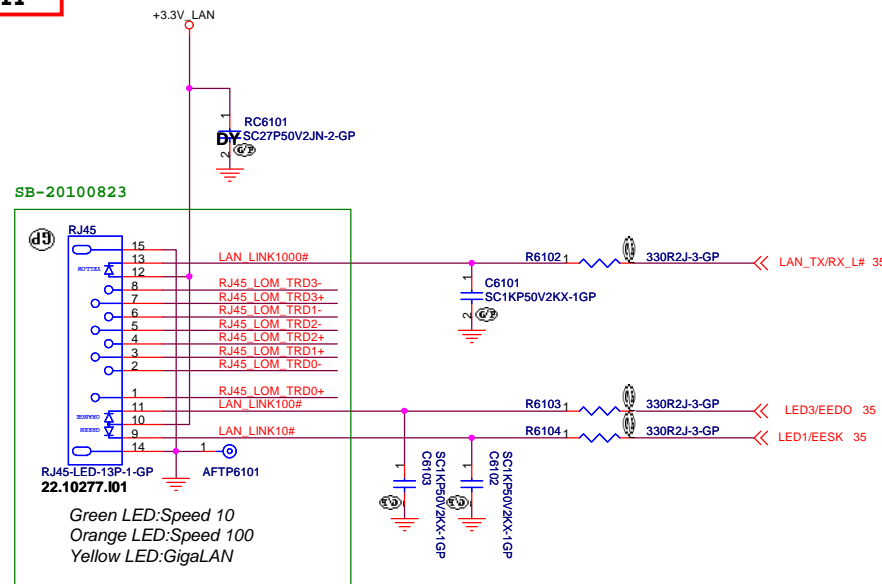
AFTP5803 1 EMC2102_FAN_TACH_1
AFTP5802 1 EMC2102_FAN_DRIVE



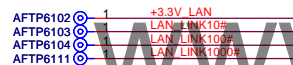
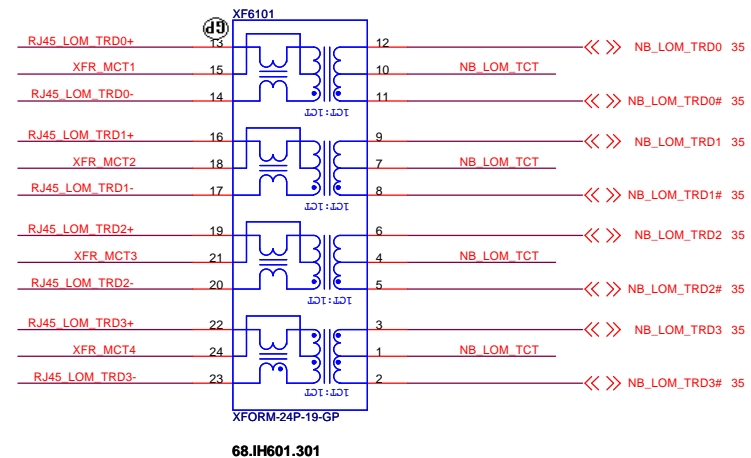
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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
FAN					
Size A4	Document Number RYU2 13 UMA				Rev A00
Date: Tuesday, September 28, 2010		Sheet 58		of 92	

SSID = LOM



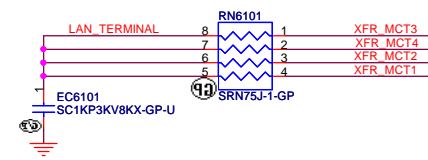
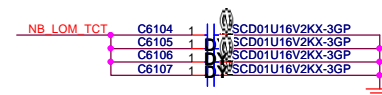
10/100/1000M Lan Transformer



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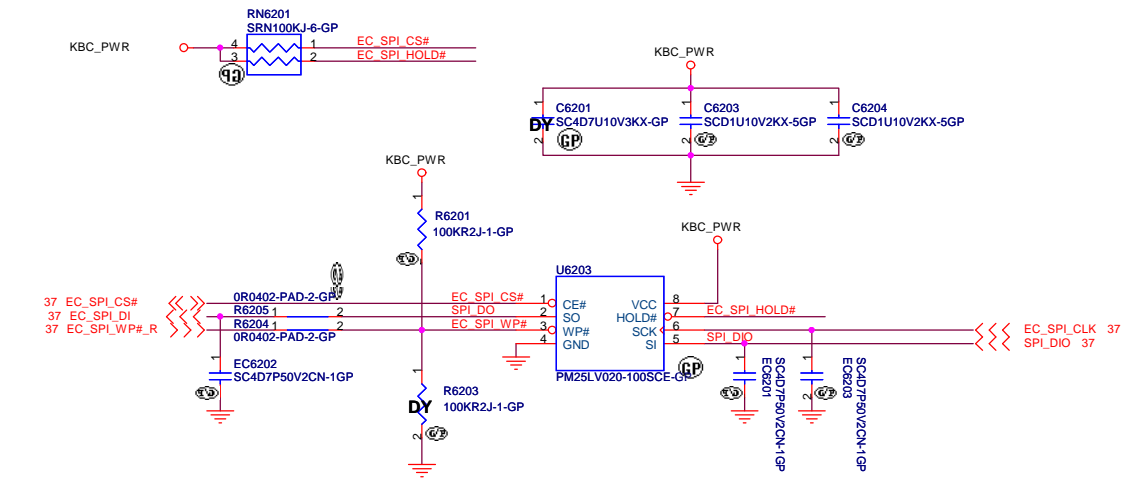
- 1.Route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.Pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

Off /No link – no light
10Mbps – Green
100Mbps – Orange
1000Mbps – Yellow (Orange/Green Combination)
Activity LED - Separate blinking yellow LED to indicate traffic

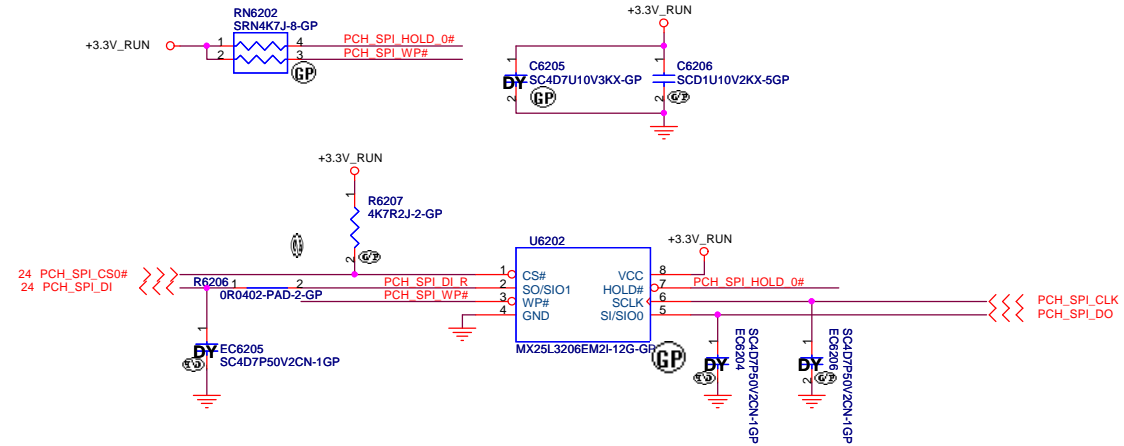


SSID = Flash.ROM

SPI FLASH ROM (2M bits) for KBC

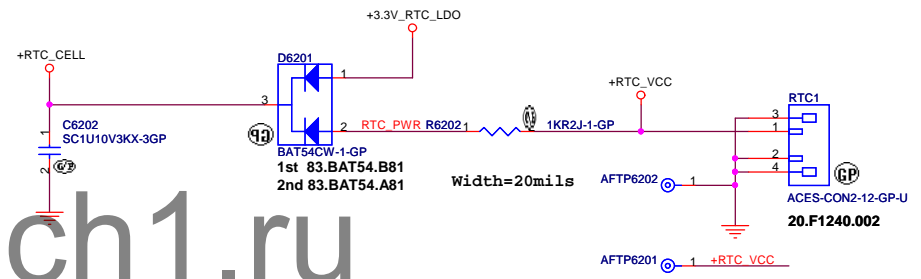


SPI FLASH ROM (32M bits) for PCH



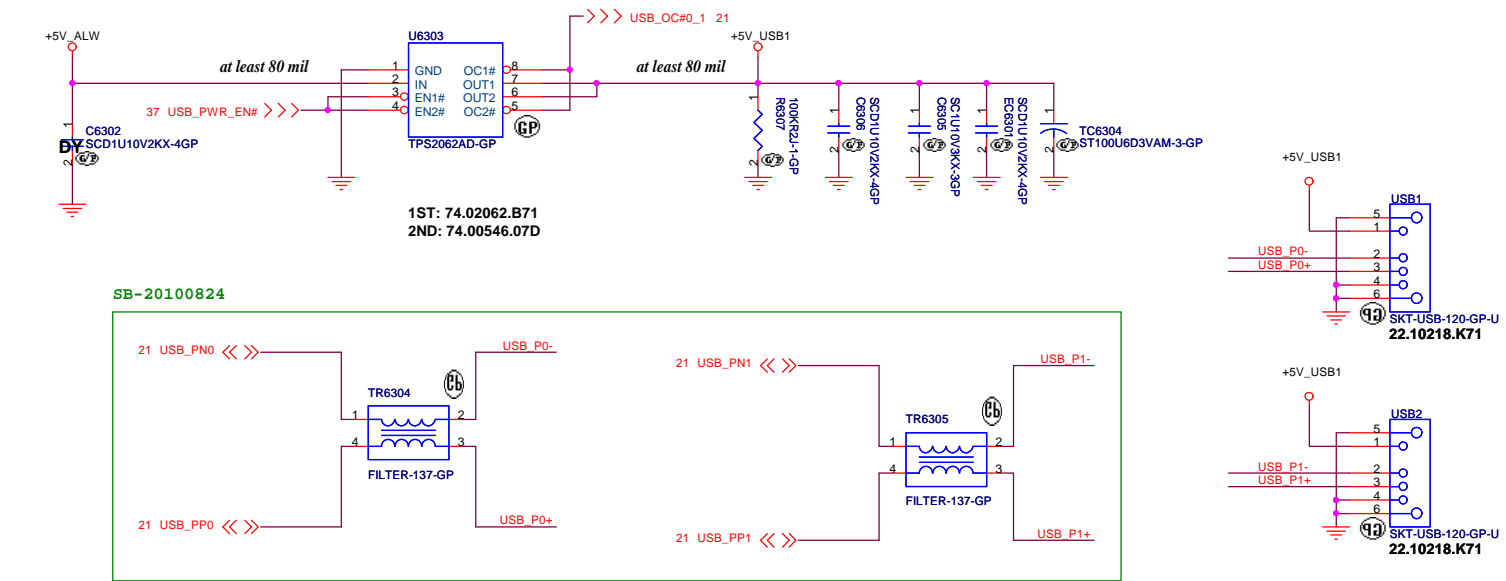
SSID = RBATT

RTC Connector



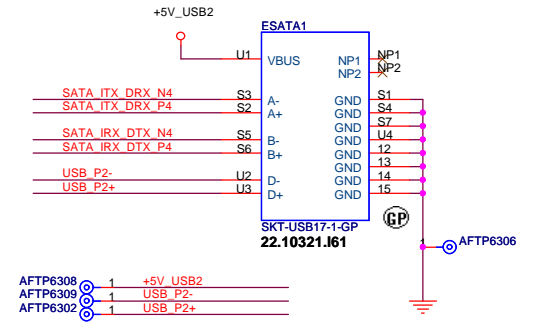
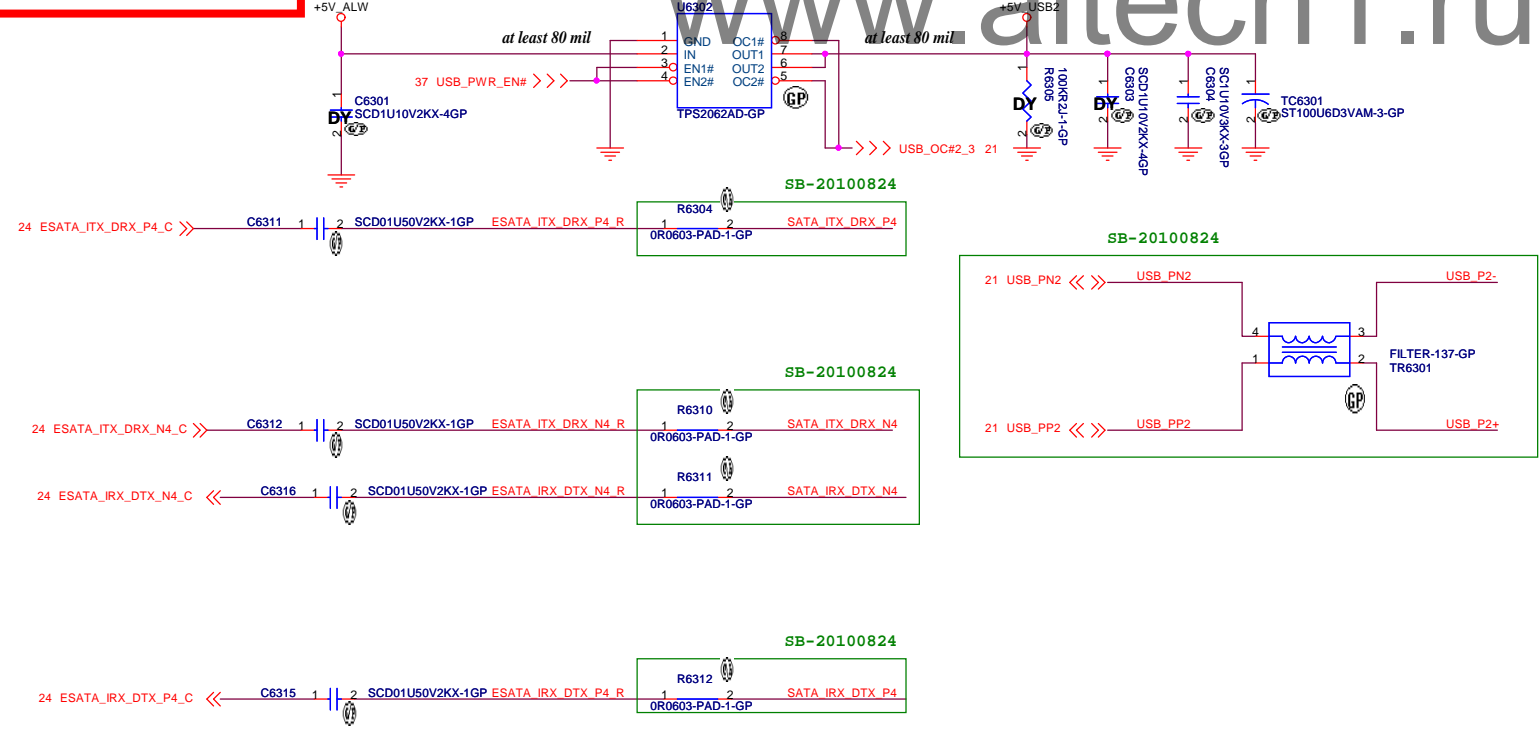
SSID = USB

USB Port Power SW



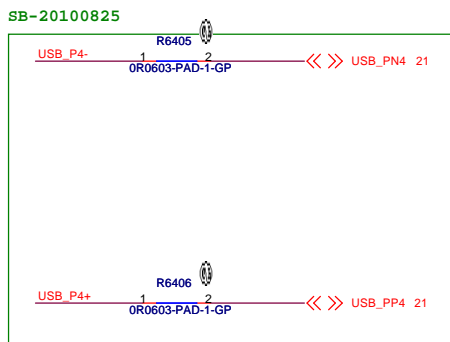
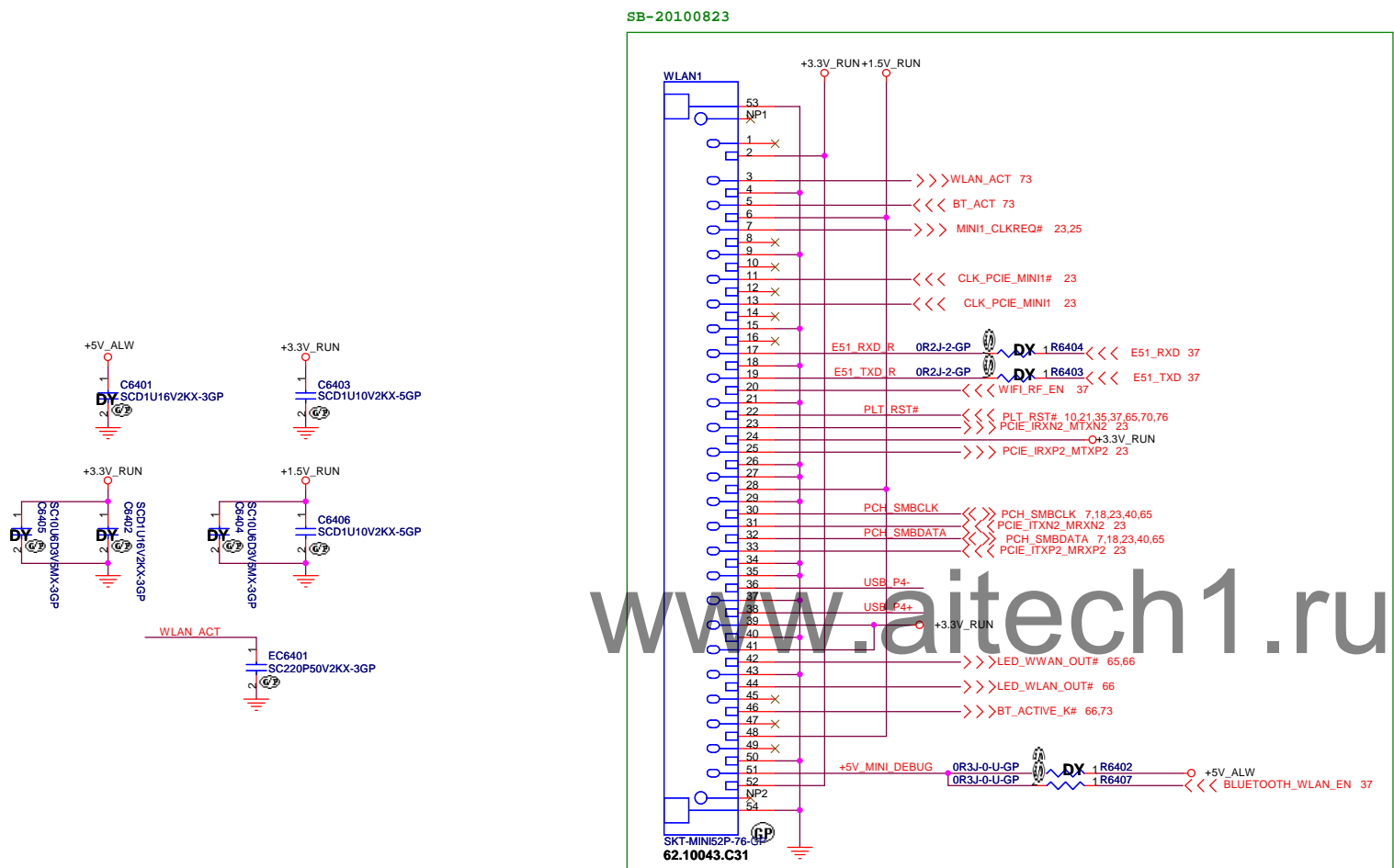
SSID = ESATA

ESATA Power



SSID = Wireless

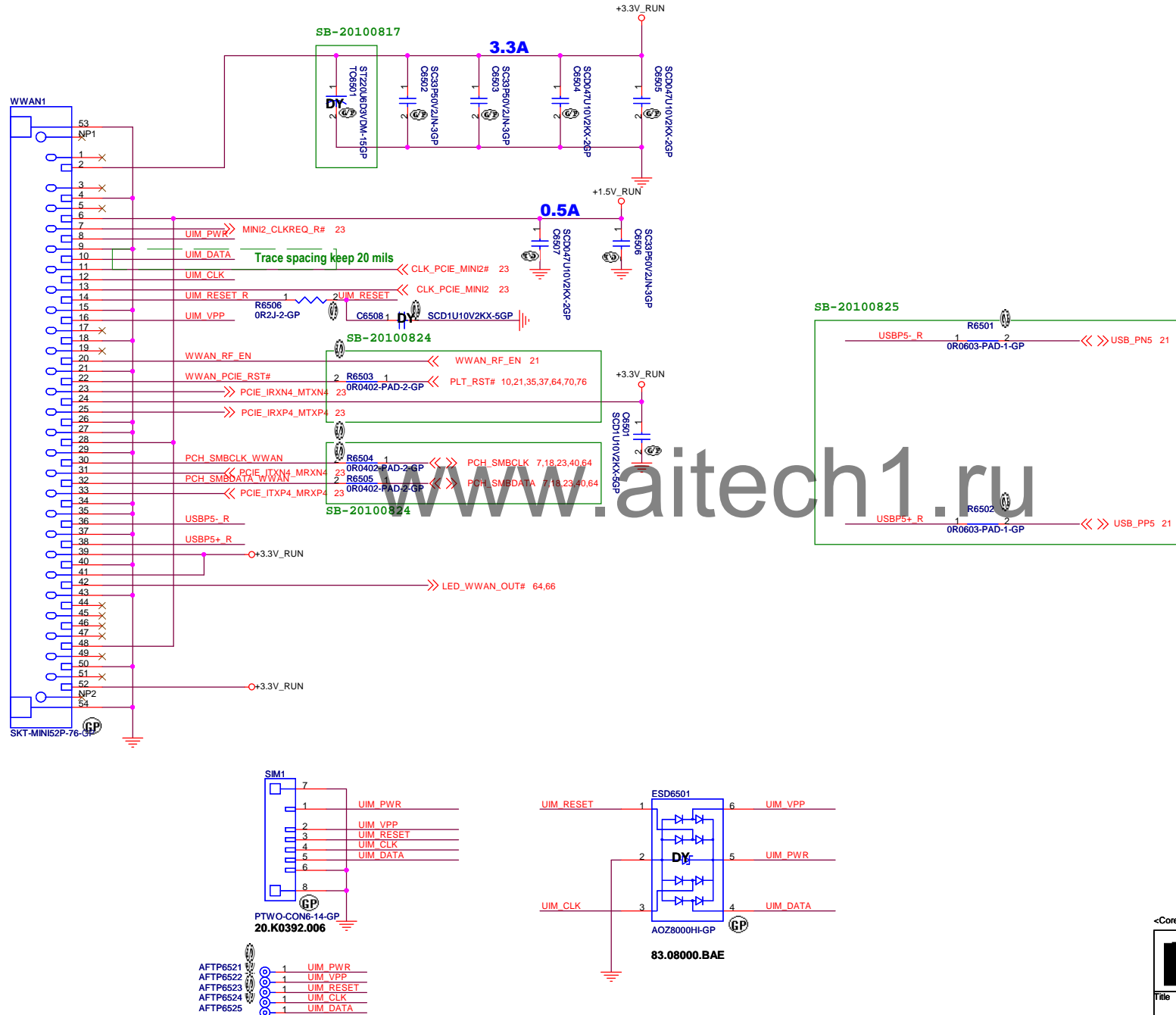
Mini Card Connector(802.11a/b/g/n)



SSID = WWAN

Layout note: Place caps C6501-C6507, TC6501 close WWAN1 connector.

MiniCard WWAN connector



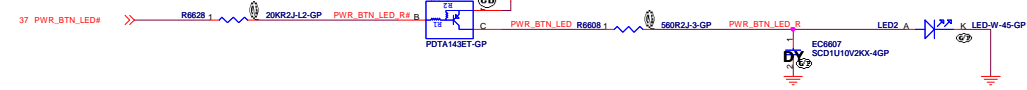
<Core Design>

SSID = LED

For LED & Capacity board:

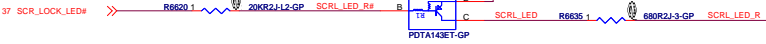
LED Type	Color	Power rail
BATTERY LED1	Amber(Multi-color)	ALW
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN/WWAN ACT LED	White	RUN

PWR BTN LED

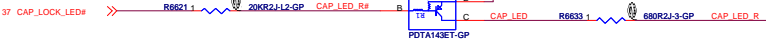


LED Board to Board

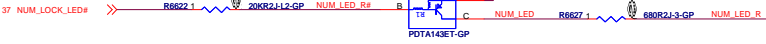
SCRLK LED



CAPS LED



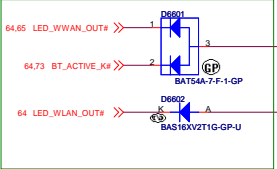
NUM LED



TOUCH PAD LED



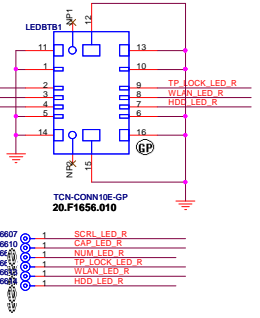
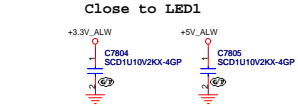
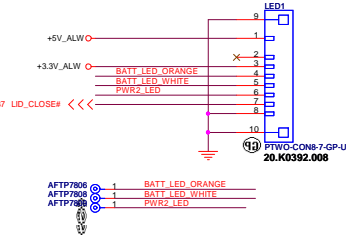
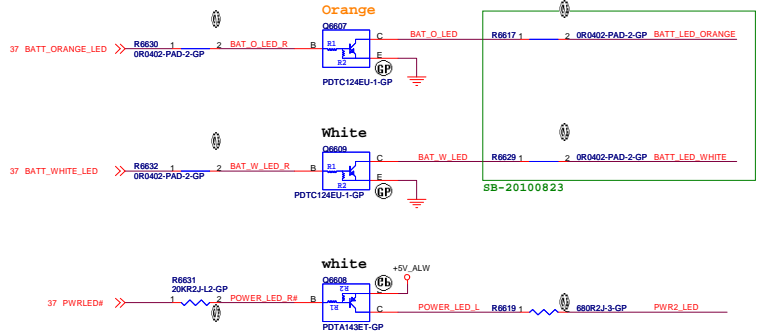
WLAN WIMAX_LED Bluetooth_LED WWAN_LED



SB-20100822



External LED



AFTP6607 1 SCRL_LED_R
AFTP6610 1 CAP_LED_R
AFTP6611 1 NUM_LED_R
AFTP6612 1 TP_LOCK_LED_R
AFTP6613 1 WLAN_LED_R
AFTP6614 1 HDD_LED_R

PTWC-CON8-7-GP-U
20.K0392.008

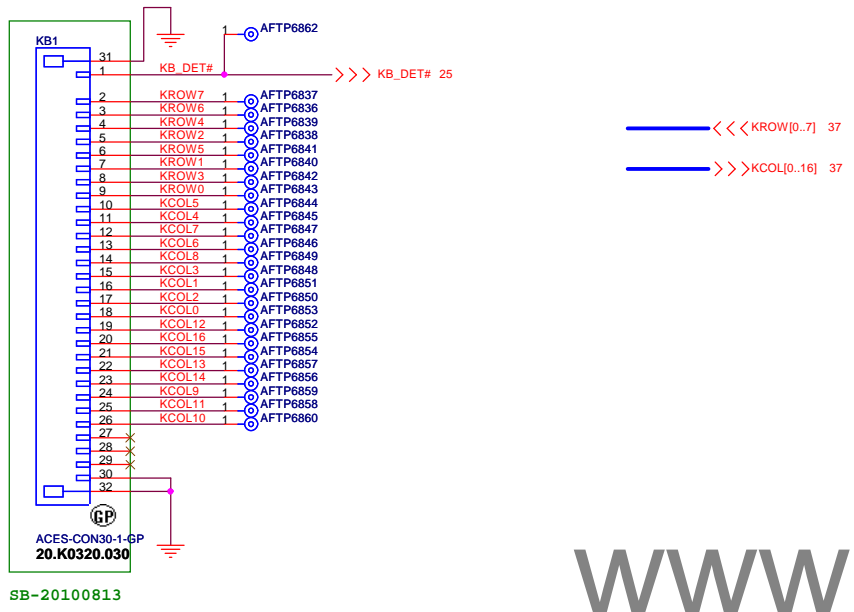
<Core Design>

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Title		
LED		
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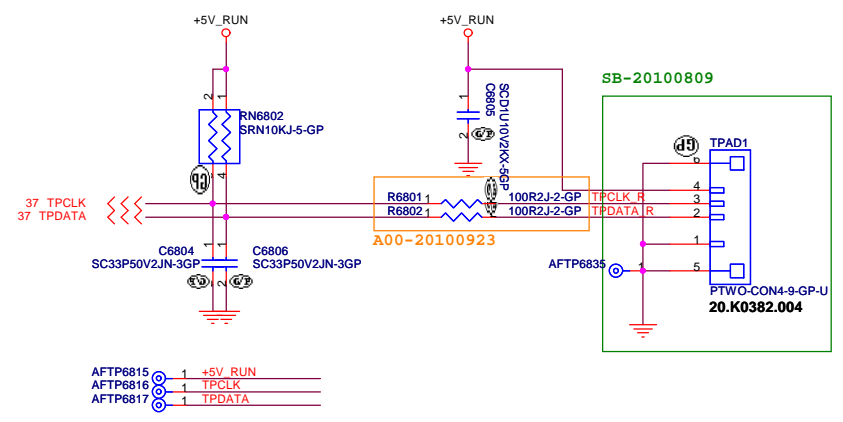
SSID = KBC

Internal KeyBoard Connector



SSID = Touch.Pad

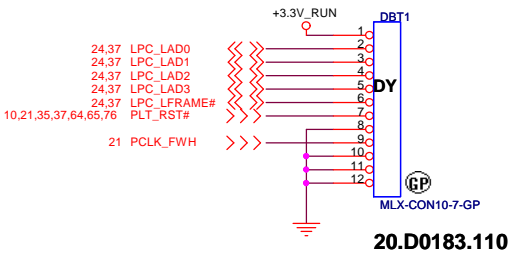
TouchPad Connector



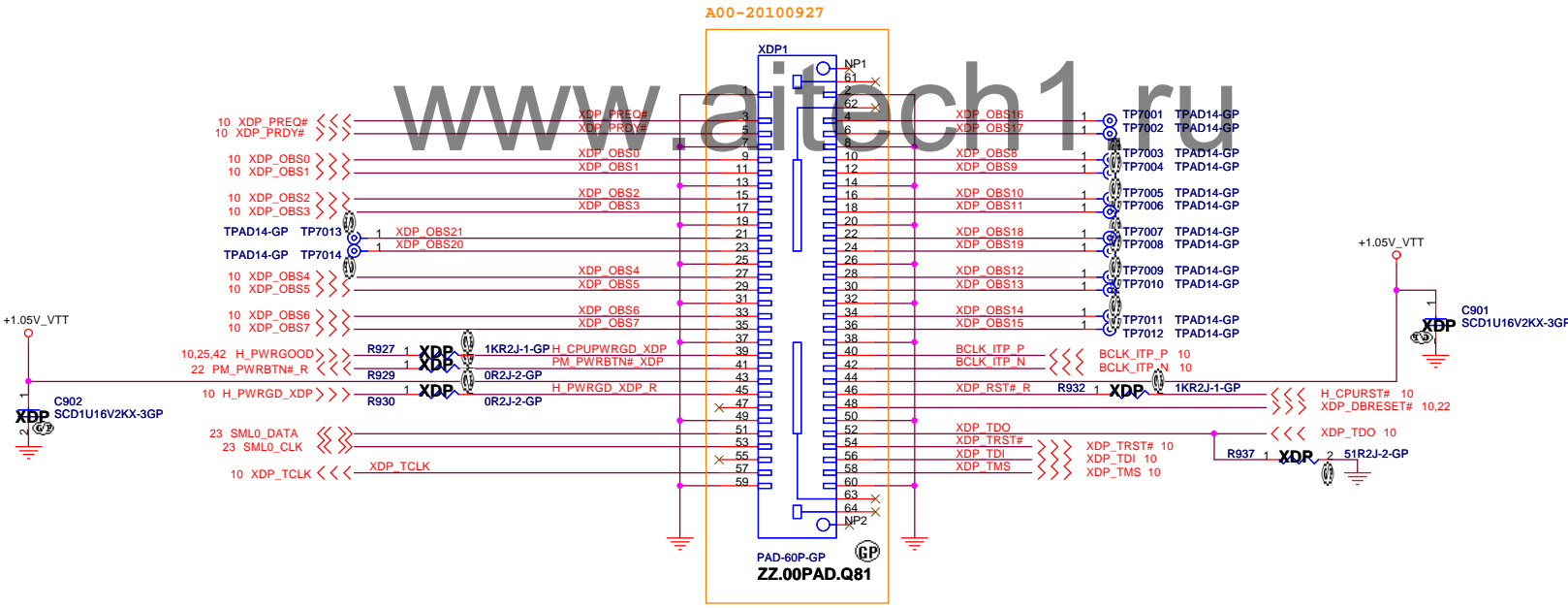
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SSID = DEBUG PORT

GOLDEN FINGER FOR DEBUG BOARD

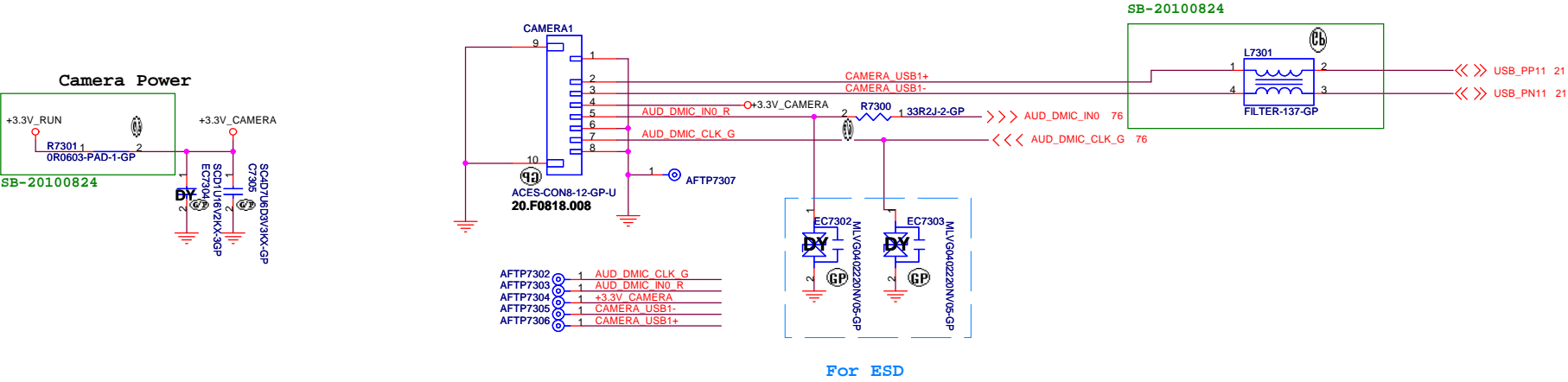


SSID = CPU



SSID = User.Interface

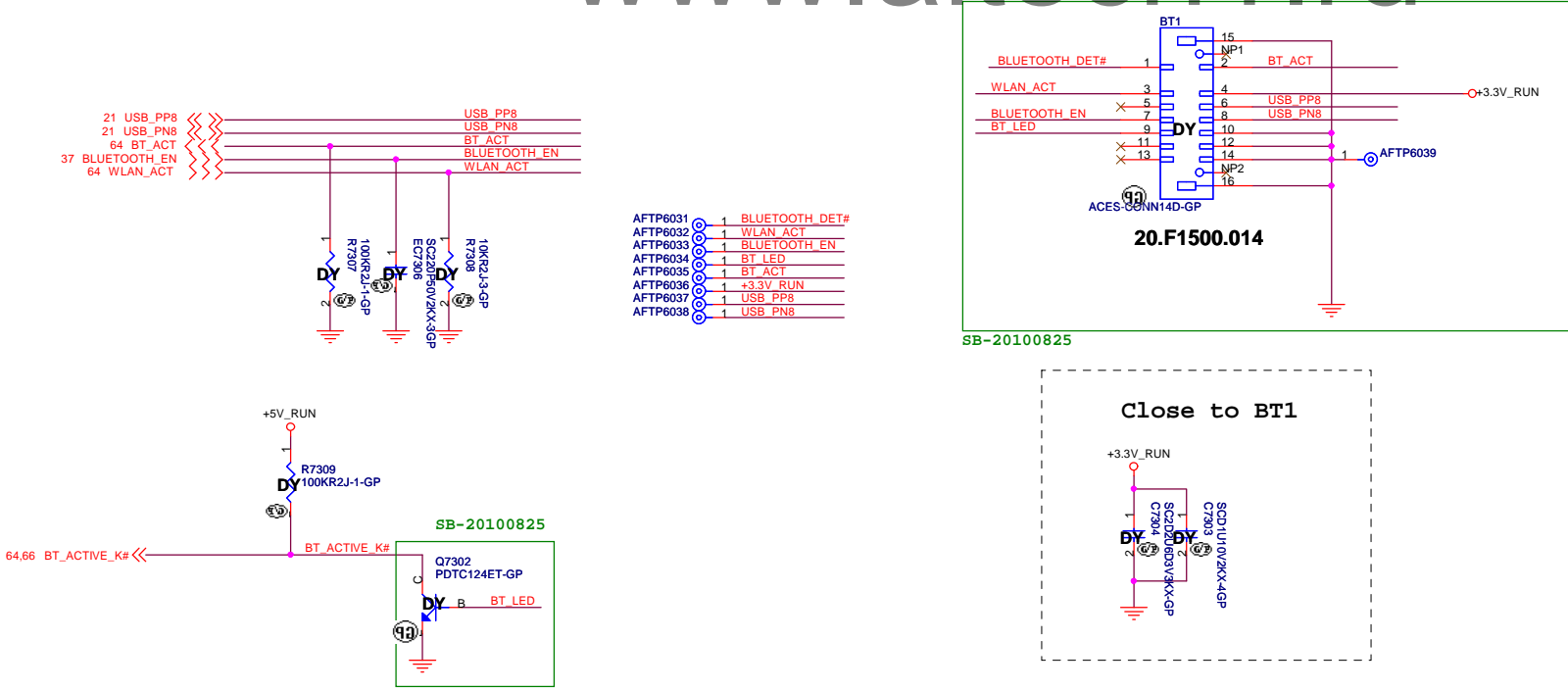
Camera Connector



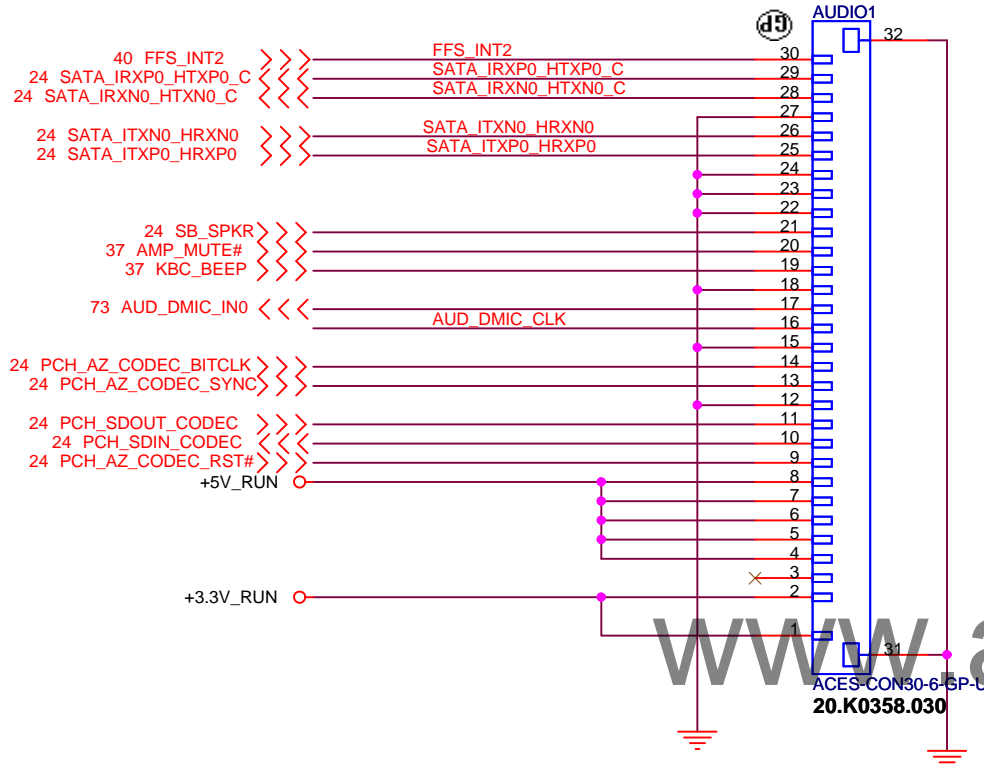
SSID = User.Interface

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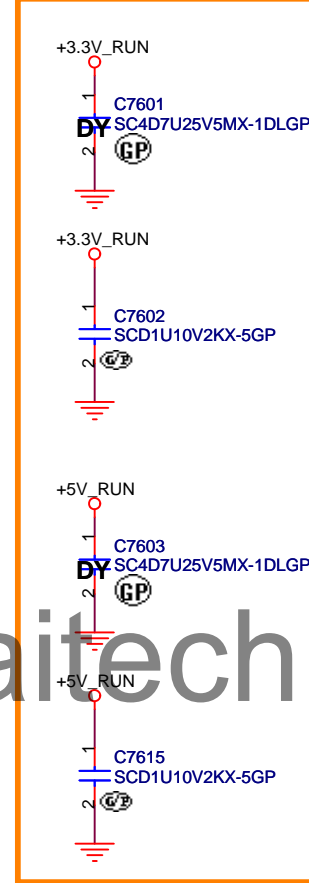
Bluetooth cable conn.



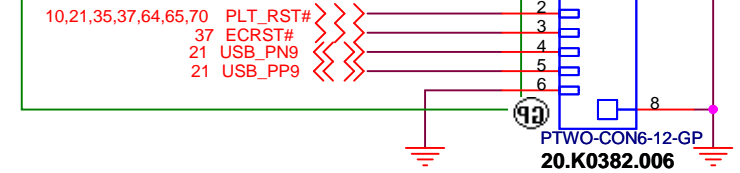
Audio board CONN



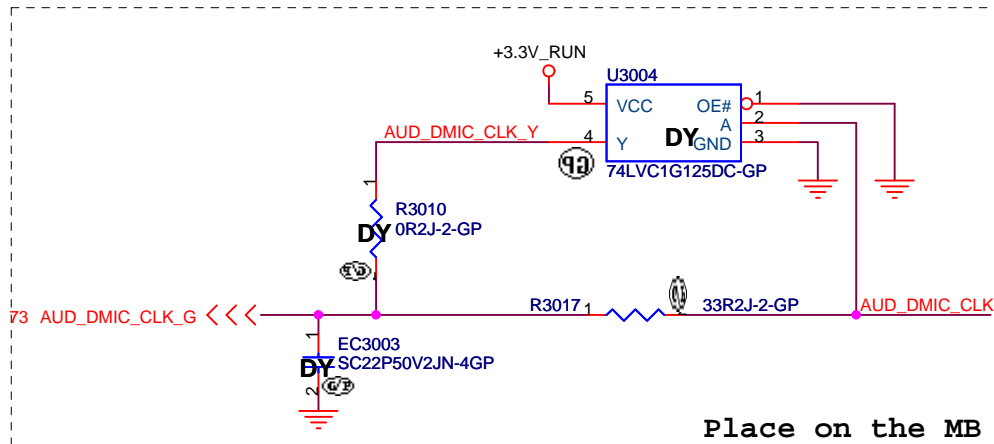
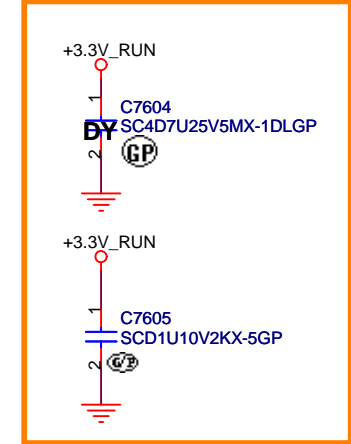
Place near AUDIO1



SB-20100817



Place near CARD1



Place on the MB

<Core Design>

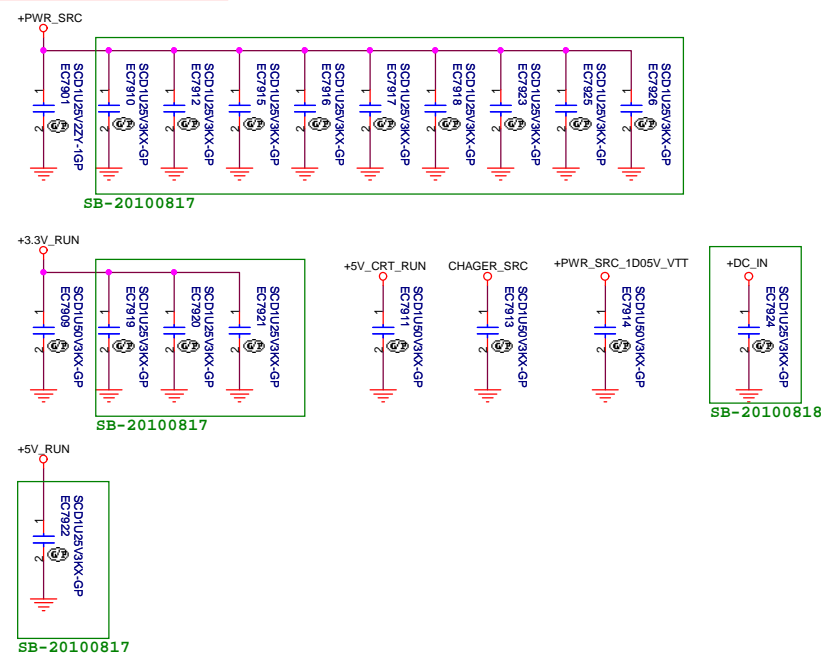


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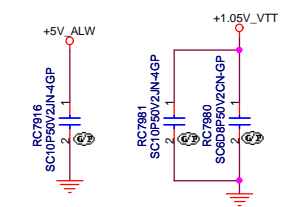
Title **DC_IN Board BTB Connector**

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SSID = EMI

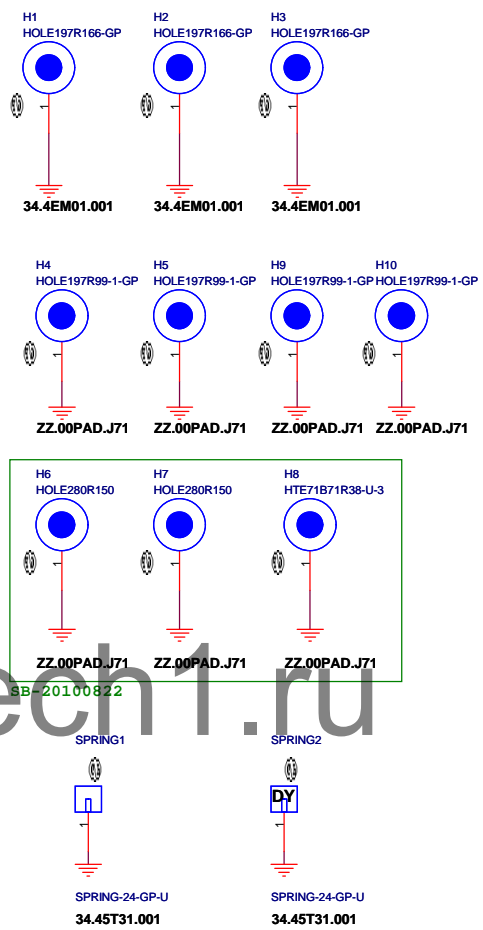


SSID = RF




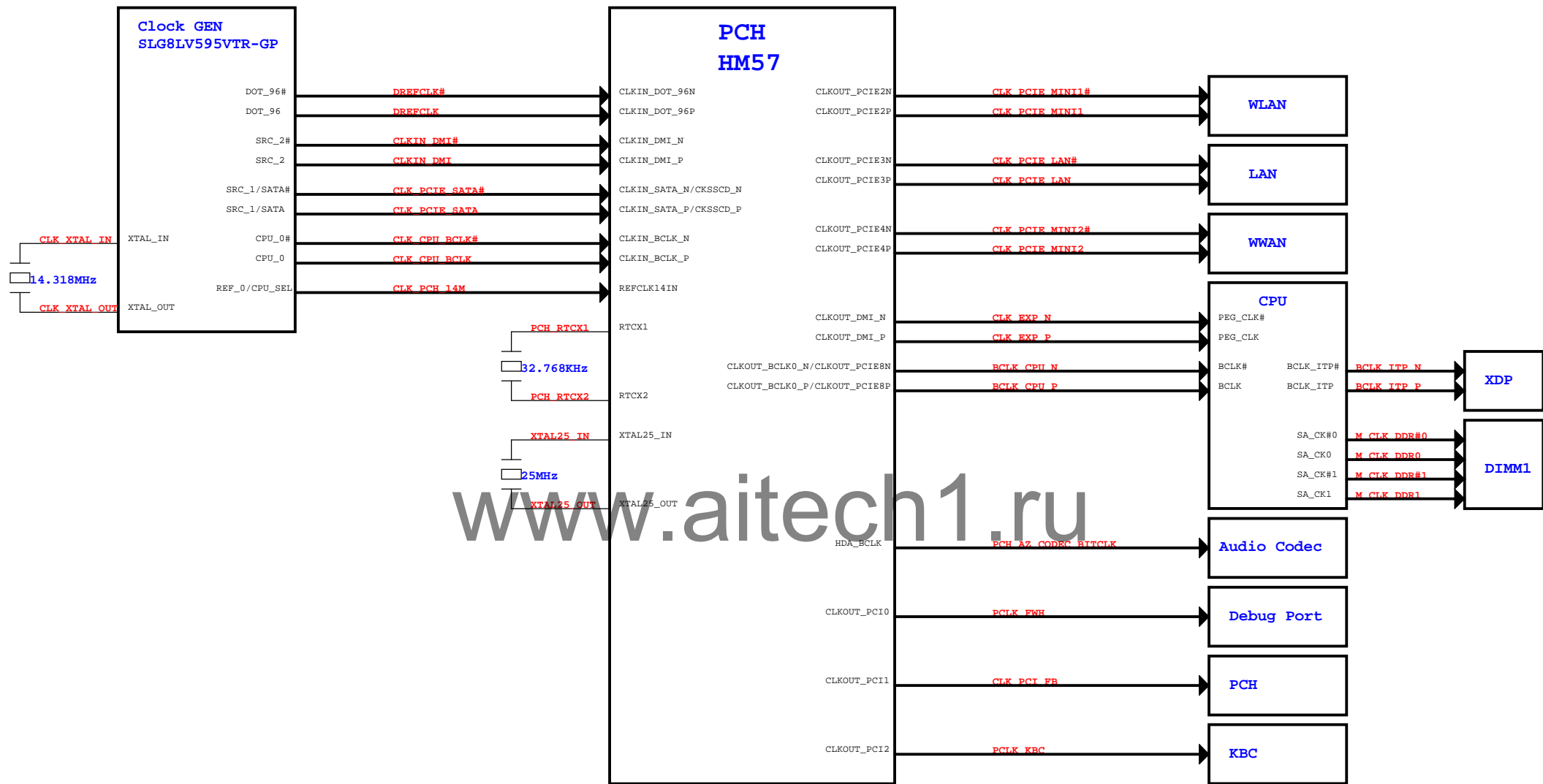
HOLE:

SSID = Mechanical



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1	43	2010/07/30	EE	+DC_IN short to GND	Modify DCIN1 connector pin4, pin5 connect to GND.	SB
2	37	2010/07/30	EE	SW1 always short to GND.	Change pin 6 connect to GND.	SB
3	68	2010/08/09	EE		Change TPAD1 pin defined.	SB
4	68	2010/08/13	EE		Change KB1 connector to 20.K0320.030.	SB
5	76	2010/08/17	EE		Add ECRST# connect to CARD1 pin 3.	SB
6	79	2010/08/17	EMI		Between +PWR_SRC and GND add 0.1uf/50v cap X 9. Between +3.3V_RUN and GND add 0.1uf/50v cap X 3. Between +5V_RUN and GND add 0.1uf/50v cap X 1. Between +DC_IN and GND add 0.1uf/50v cap X 1. Between +DC_IN and GND add 0.1uf/50v cap.	SB
7	47	2010/08/18	Power		Change +VCC_CORE VID3~5 from 001 to 010.	SB
8	37	2010/08/19	EE		Add LID_CLOSE# pull high resistor to +3.3V_ALW.	SB
9	51	2010/08/19	EE		Co-lay +1.8V_RUN LDO power solution.	SB
10	55	2010/08/19	EE		Between +5V_RUN and +5V_CRT_RUN add Fuse.	SB
11	45	2010/08/22	ME		Change PC4532, PC4530, PC4533 from 1206 size to 0805 size for ME request.	SB
12	45	2010/08/22	Power		Change PU4505 from SIS7716 to SIS412DN (84.00412.037). For cost down.	SB
13	47	2010/08/22	Power		PR4714 change to 2.2K for OTP & OCP setting. PR4715 change to 4.7K for OTP & OCP setting. PR4716 change to 7.15K for OTP & OCP setting. PR4721 change to 78.7K for Load Line & COMP setting. PC4705 change to 27pF for Load Line & COMP setting. PR4728 change to 63.4K for Current Monitor setting. PC4709 change to 22nF for Current Monitor setting.	SB
14	66	2010/08/22	EE		Add D6601, D6602 for wireless function.	SB
15	7	2010/08/23	RF		Add RC701, RC702 for RF request.	SB
16	42	2010/08/23	EE		Change +1.5V_CPU power rail from +1.5V_RUN to +1.5V_SUS.	SB
17	53	2010/08/23	Power		PR5314 :7.5k change to 8.45K(64.84515.6DL) for GFX core imon.	
18	61	2010/08/23	EE		Change RJ45 connector to 22.10277.I01 for hi-port fail.	SB
19	64,65	2010/08/23	EE		Change WLAN1, WWAN1 connector to 62.10043.C31.	SB
					<div> <div>Core Design</div> <div>  <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div> </div> <div> <div>Title</div> <div>Change List(1/3)</div> <div> <div>Size A3</div> <div>Document Number RYU2 13 UMA</div> <div>Rev A00</div> </div> <div> <div>Date: Tuesday, September 28, 2010</div> <div>Sheet 88 of 89</div> </div> </div> </div>	



Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
20	66	2010/08/23	EE		Change R6617, R6629 to 0ohm.	SB
21	63,73	2010/08/24	EMI		Change USB port0, port1, port2 and camera from 0 ohm to common chock.	SB
22	73	2010/08/25	EE		Dummy BT 365 function.	SB
23	24	2010/08/25	EE		Change C2402 from 12PF to 5PF.For Vendor recommend. Change C2403 from 12PF to 6PF.For Vendor recommend.	SB
24	7	2010/08/25	EE		Change C714, C715 from 12PF to 15PF for vendor recommend.	SB
25	47,49	2010/08/25	Power	SI7686DP-T1-GE3-GP will EOL.	PU4702, PU4703, PU4902: (SI7686DP-T1-GE3-GP) change to SIR172DP-T1-GE3-GP 84.00172.037	SB
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1	7	2010/08/24	EE	Cost down	Change R708, R709, RN701, RN702, RN703, RN704 from 0 ohm to short pad.	SB
2	10	2010/08/23	EE	Cost down	Dummy U927, R989, R977, Q901, C915, R934, R989. Add R935, R919. Change R920 to 3 K ohm.	SB
3	10	2010/08/24	EE	Cost down	Change R906, R909, R921, R924, R926 from 0 ohm to short pad.	SB
4	20	2010/08/24	EE	Cost down	Change R2011 from 0 ohm to short pad.	SB
5	21	2010/08/24	EE	Cost down	Change R2104, R2121 from 0 ohm to short pad.	SB
6	21	2010/08/24	EE	Cost down	Change R2519, R2102, R2105 from single resistor to array resistor.	SB
7	22	2010/08/24	EE	Cost down	Change R2207, R2210, R2218, R2213, R2216, R2219, R2220, R2211, R2212 from 0 ohm to short pad.	SB
8	23	2010/08/24	EE	Cost down	Change RN2311, RN2312, RN2314 from 0 ohm to short pad.	SB
9	23	2010/08/24	EE	Cost down	Change R2302, R2201, R2301, R2209 from single resistor to array resistor.	SB
10	24	2010/08/24	EE	Cost down	Change R2417 from 0 ohm to short pad.	SB
11	25	2010/08/24	EE	Cost down	Change R2521, R2334, R2522, R2512, R2411, R2513, R2217, R2538, R2304, R2533, R2416, R2503, R2535, R2214 from single resistor to array resistor.	SB
12	26	2010/08/24	EE	Cost down	Change R2606, R2605, R2601, R2609, R2602 from 0 ohm to short pad.	SB
13	27	2010/08/24	EE	Cost down	Change R2707 from 0 ohm to short pad.	SB
14	35	2010/08/24	EE	Cost down	Change R3509, R3512, R3508, R3514 from 0 ohm to short pad.	SB
15	35	2010/08/24	EE	Cost down	Change R3517, R3518 from single resistor to array resistor.	SB
16	37	2010/08/24	EE	Cost down	Change R3706, R3730, RR3720, R3707, R3753, R3702, R3723, R3727 from 0 ohm to short pad.	SB
17	37	2010/08/24	EE	Cost down	Change R3742, R3743 from single resistor to array resistor.	SB
18	39	2010/08/24	EE	Cost down	Change R3910, R3906 from single resistor to array resistor.	SB
19	44	2010/08/24	EE	Cost down	Change R4401 from 0 ohm to short pad.	SB
					<div><Core Design><div><div>DELL</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div><div>Title<div>Change List(1/3)</div></div><div>Size<div>A3</div>Document Number<div>RYU2 13 UMA</div>Rev<div>A00</div></div><div>Date: Tuesday, September 28, 2010Sheet 91 of 89</div></div>	

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20	45	2010/08/24	EE	Cost down	Change PR4522, PR4515, PR4530, PR4531, PR4533, PR4524 from 0 ohm to short pad.	SB
21	46	2010/08/26	EE	Cost down	Dummy PU4606, PD4605, PR4623, PR4624, PR4625.	SB
22	47	2010/08/24	EE	Cost down	Change PR4719, R4710, PR4701, PR4702, PR4703, PR4704, PR4705, PR4707, PR4708 from 0 ohm to short pad.	SB
23	49	2010/08/24	EE	Cost down	Change PR4924 from 0 ohm to short pad.	SB
24	50	2010/08/24	EE	Cost down	Change PR5014, PR5002 from 0 ohm to short pad.	SB
25	53	2010/08/24	EE	Cost down	Change PR5302, PR5303, PR5304, PR5305, PR5307, PR5308, PR5309, PR5310, PR5331, PR5332, PR5333 from 0 ohm to short pad.	SB
26	54	2010/08/24	EE	Cost down	Change R5415, R5414 from 0 ohm to short pad.	SB
27	63	2010/08/24	EE	Cost down	Change R6304, R6310, R6311, R6312 from 0 ohm to short pad.	SB
28	64	2010/08/25	EE	Cost down	Change R6405, R6406 from 0 ohm to short pad.	SB
29	65	2010/08/24	EE	Cost down	Change R6503, R6504, R6505, R6501, R6502 from 0 ohm to short pad.	SB
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